

[RESEARCH]

Room-Temperature Single Electron Devices by Scanning Probe Process

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A single electron transistor (SET) and a single electron memory were fabricated using the improved pulse-mode AFM nano-oxidation process. A single electron transistor which works as an electrometer for detecting the potential of the memory node of the single electron memory showed the clear Coulomb oscillation characteristics with the periods of 2.1V at room temperature. A single electron memory showed the hysteresis loop by the return trip of the memory bias when starting from 0V to 10V and again coming back to 0V.

§1 Introduction

A various types of single electron transistors and memories were, so far, studied. Almost all single electron devices so far studied adopted the self-organized nano-structure because of the difficulty of the artificial fabrication process of the nano-structure. The some examples of the self-organized nano-structure for the single electron devices are the polycrystalline silicon film¹⁾, the poly-crystal silicon dot²⁾, and the squeezed delta-doped GaAlAs/GaAs layer³⁾ for the multi-tunnel junctions and/or memory node. They showed the clear single electron device characteristics such as the digitized threshold voltage shifts¹⁾ or hysteresis loop³⁾ by the injected few number of electrons. Those devices, however, include the problem of the poor reproducibility of the device characteristics because of the application of the spontaneously formed nano-structures. On the other hand, in the present paper, we show the new device fabrication process⁴⁻⁶⁾, which could artificially fabricate the few tens of nano-meter order small structure and room temperature operated single electron transistor and single electron memory were realized.

§2 AFM nano-oxidation process

The new fabrication process used the atomic force microscopy (AFM) cantilever as an ultra small cathode, and pulse bias was applied between cantilever and the 2.5nm thick titanium (Ti) thin film that was on the atomically flat α -Al₂O₃ substrate as shown in **Fig. 1**. AFM nano-oxidation process so far we proposed used DC bias between the cantilever and the titanium metal, and the

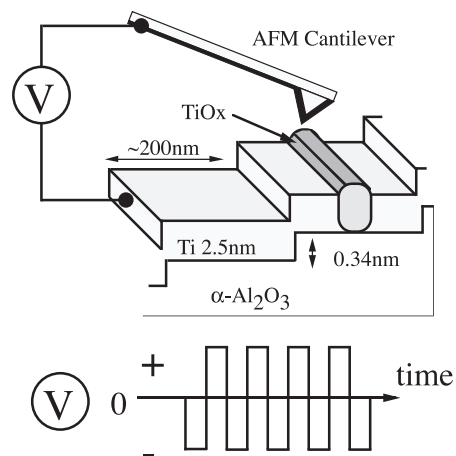


Fig.1 Schematic diagram of pulse-mode AFM nano-oxidation process on atomically flat α -Al₂O₃ substrate.

surface of the Ti metal was anodized to form the oxidized titanium line (TiOx) which works as a tunnel junction for the single electron devices⁴⁻⁶. During this DC-mode AFM nano-oxidation process, however, the positive hydrogen ions H⁺ formed the space charge at the front end of the TiOx/Ti interface, which prevents the further oxidation. This causes the difficulty for the deeper oxidation. In order to solve the problem, the $\pm 1.5\sim 2V$ pulse bias was applied instead of the DC bias between the conductive AFM cantilever and the Ti metal⁷. The negative pulse anodized the surface of the metal and the positive pulse neutralized the positive

space charge from the front end of TiOx. Therefore, using the pulse bias for the oxidation, the deeper oxidation becomes possible than the DC bias do at the same applied bias. In another words, a narrower and deeper oxidized Ti line could be formed using the lower applied pulse bias. **Fig. 2** shows the AFM image of the TiOx line folded six times on the atomically flat Ti/ α -Al₂O₃ substrate fabricated by the present new AFM nano-oxidation process. The line width is 20 nm, and line height 1.2 nm. The smooth and uniform TiOx line was obtained reproducibly. Using this new process, the single electron transistor and the single electron memory were fabricated.

§3 Single electron transistor

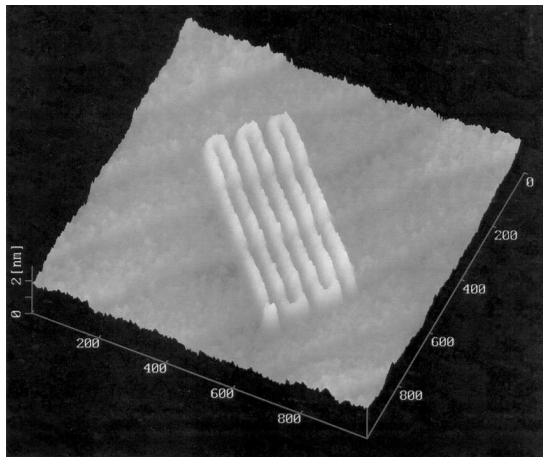


Fig.2 AFM image of TiOx line folded six times on atomically flat Ti/ α -Al₂O₃ substrate made by pulse-mode AFM nano-oxidation. Linewidth is 20 nm, and line height 1.2 nm.

Fig. 3 shows the schematic structure and AFM image of the fabricated one island side gate single electron transistor (SET) on the atomically flat α -Al₂O₃ substrate. Using the pulse mode AFM nano-oxidation process, two tunnel junctions for SET were formed by TiOx lines. The size of the tunnel junction is 19nm(width) x 26nm(length) x 2nm(thickness) and island size 8nm x 26nm. The width of the gate insulator for the side gate SET was increased up to 964 nm to completely prevent the gate leakage current at room temperature (In the previous work, the width of the gate insulator was 300nm).

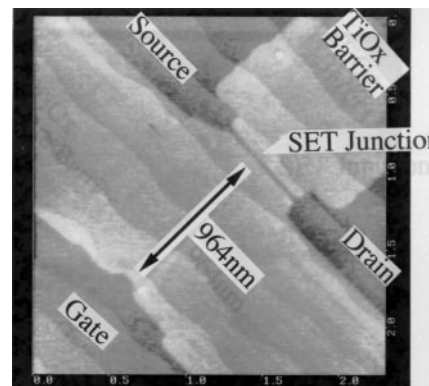
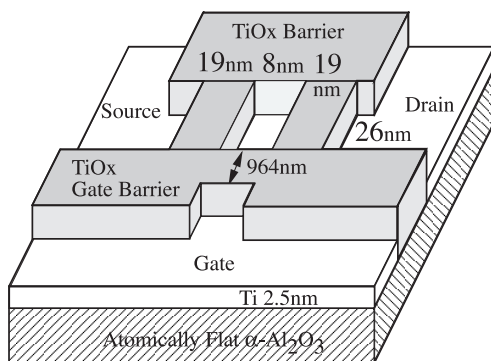


Fig.3 Schematic structure and plain AFM image of the fabricated one island side gate SET on the atomically flat substrate. Two tunnel junction size is 19nm(width) x 26nm(length) x 2nm(thickness) and island size 8nm x 26nm.

Fig. 4 shows the drain current-gate bias characteristics of the SET at room temperature using the drain bias as a parameter. The drain current of the SET oscillates with the period of 2.1V at room temperature in the gate bias range of 0V to 10V at the drain bias of $V_D=0.25V$ and 0.3V. Five peaks are clearly seen for the each drain bias condition. The current modulation rate is from 20% to 30%. Even at the different drain bias, the drain current shows the oscillation peaks at the same gate bias points. The gate capacitance estimated from the periods of the Coulomb oscillation is $8 \times 10^{-20}F$. **Fig. 5** shows the drain current-gate bias characteristics when the gate bias was changed from -10V to 10V at the drain bias of $V_D=0.25V$. The peaks of the Coulomb oscillation appear periodically and symmetrically against the

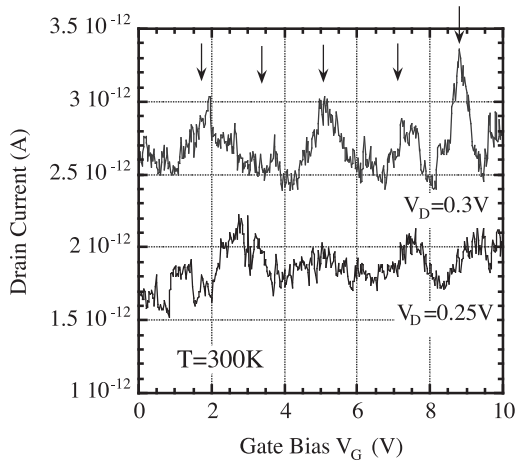


Fig. 4 Dependence of Coulomb oscillation on drain bias at room temperature.

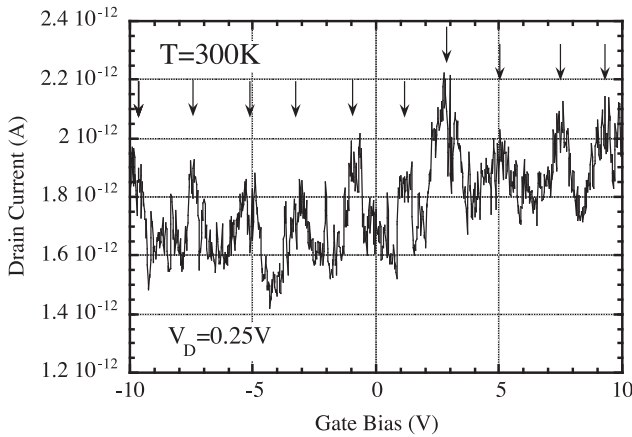


Fig. 5 Symmetrical characteristics of Coulomb oscillation against gate bias at room temperature.

plus and minus region in the gate bias.

Thus, the fabricated SET shows the clear gate action even at room temperature.

§4 Single electron memory

Fig. 6 shows the equivalent circuit of the single electron memory which consists of the multi-tunnel junction and the normal memory capacitance. The memory node of the single electron memory where few number of electrons are stored is connected by the single electron transistor (SET) through the normal capacitance C_g . Using the equivalent circuit of the single electron memory shown in Fig. 6, the principle of the operation of the single electron memory is explained as follows. By increasing the memory bias, V_{MEM} , the potential of the memory node V_t also increases in proportion to the ratio of the memory capacitance C_{gt} and the multi-tunnel junction capacitance, C_{tt} , i.e.,

$$V_t = V_{MEM} C_{gt} / (C_{tt} + C_{gt}). \tag{1}$$

When the potential of the memory node V_t becomes larger than the Coulomb gap bias of the multi-tunnel junction V_0 , one electron can pass through the multi-tunnel junction to reach the memory node, which lowers the potential of the memory node as $e / (C_{tt} + C_{gt})$, and the second electron can not pass through the multi-tunnel junction. By increasing the memory bias fur-

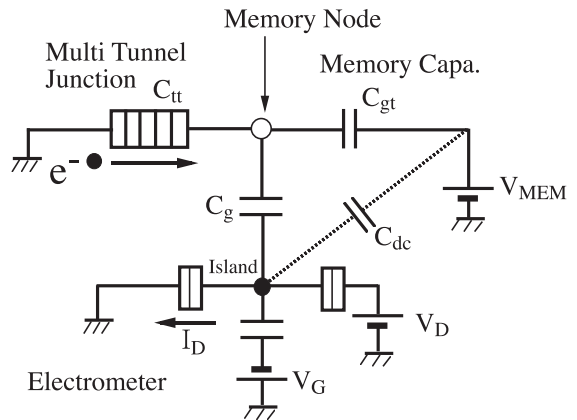


Fig. 6 Equivalent circuit of single electron memory.

ther, the potential of the memory node V_t again reaches to the Coulomb gap bias, V_0 then the second electron can pass through the multi-tunnel junction to reach the memory node. Thus the one by one electron transfer becomes possible through the multi-tunnel junction to the memory node. When the n electrons are stored at the memory node, the potential of the memory node which is lowered by n electrons is described as follows:

$$V_t = (V_{MEM} C_{gt} - ne) / (C_{tt} + C_{gt}), \quad (2)$$

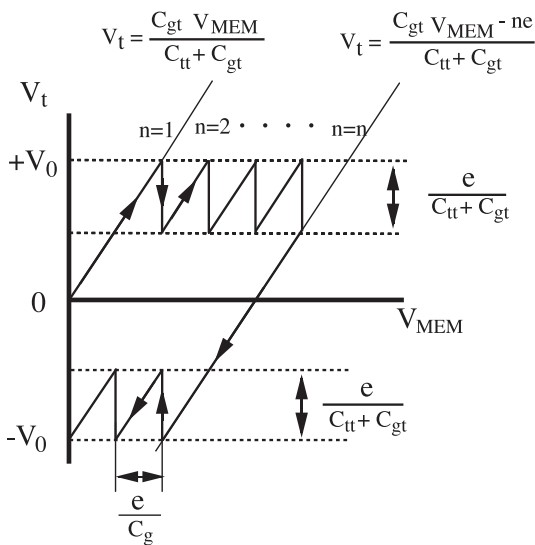


Fig. 7 Dependence of memory node potential, V_t , on memory bias, V_{MEM} .

where e is the electron charge. When the memory bias, V_{MEM} comes back to the lower bias, the potential of the memory node V_t goes into the negative region because of the stored n electrons. When V_t becomes smaller than the negative Coulomb gap bias of the multi-tunnel junction $-V_0$, the electron is ejected one by one to the ground. Therefore, the potential of the memory node V_t shows the hysteresis loop. The relation between the memory node potential V_t and the memory bias V_{MEM} is shown in Fig. 7. Thus, few number of electrons are memorized at the memory node for few hundred seconds and this device works as a single electron memory. The change of the potential at the memory node by the injection and the ejection of electrons through the multi-tunnel junction is detected by the change of the drain current of the SET, which works as an electrometer. The change of the drain current of the electrometer is considered to be linearly proportional to the potential change of the memory node.

Fig. 8 shows the schematic structure of the fabricated single electron memory which sits on the atomically flat α - Al_2O_3 substrate. Fig. 9 is the AFM image of the multi-tunnel junction area and two tunnel SET junctions of the fabricated single electron memory. The device consists of the multi-tunnel junction and normal capacitance for the memory and two tunnel junctions for the single electron transistor. There are four electrodes, i.e., the memory bias electrode for the memory,

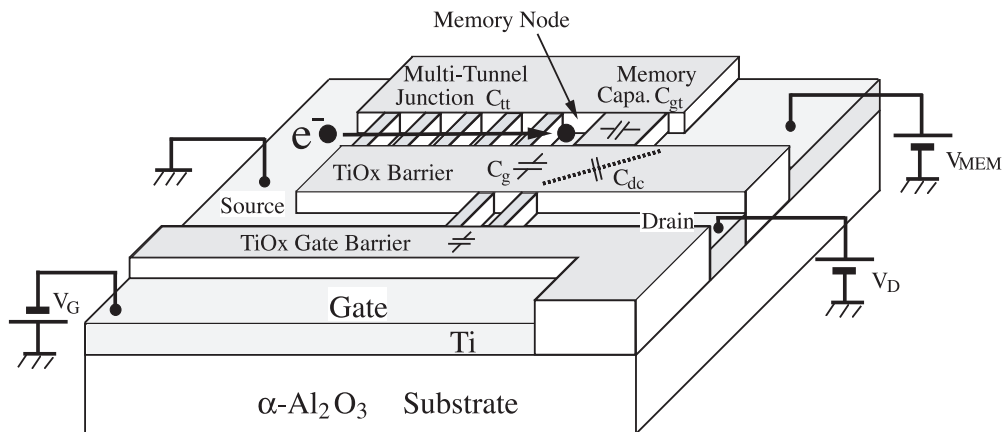


Fig. 8 Schematic structure of single electron memory on atomically flat α - Al_2O_3 substrate made by pulse-mode AFM nano-oxidation process.

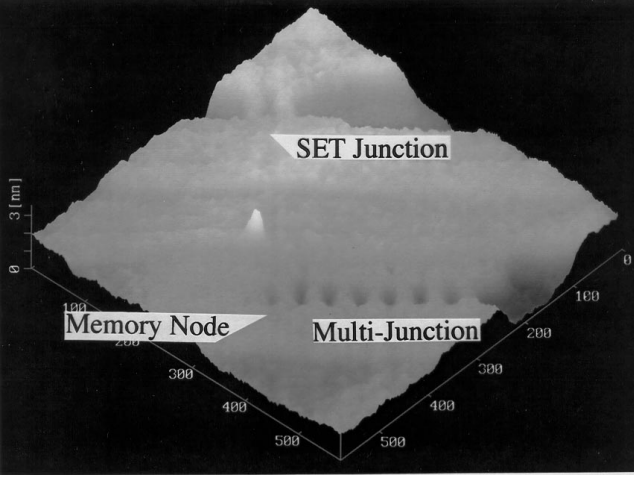


Fig.9 Plain AFM image of the fabricated single electron memory on atomically flat substrate. Multi-tunnel junctions for memory and SET junctions for electrometer are seen

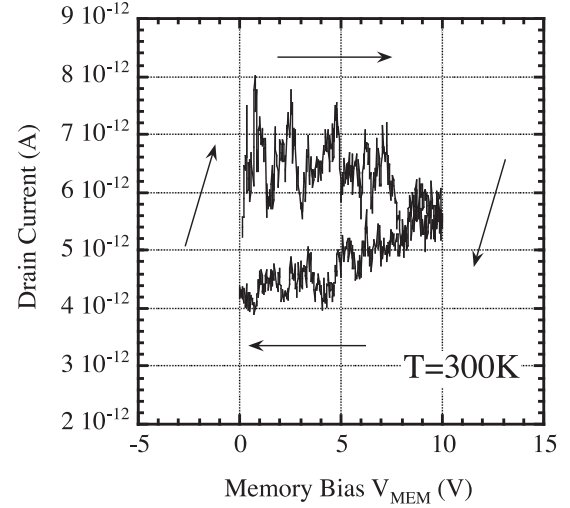


Fig.10 Hysteresis loop of single electron memory at room temperature. Gate bias and drain bias for SET were set at $V_G=1.5V$ and $V_D=3V$, respectively. Memory bias was applied from $V_{MEM}=0V$ to $10V$ and back to $0V$.

the source, drain and gate electrodes for the single electron transistor. The multi tunnel junction consists of five or seven tunnel junctions which are $15\sim 25nm$ in width, $15\sim 25nm$ in length, $2nm$ in thickness, and the spacing between them is $10\sim 15nm$. The normal memory capacitance is $341nm$ in width and $15\sim 25nm$ in length, and $2nm$ in thickness. The area between the multi-tunnel junction and the memory capacitance is designated as a memory node where few number of electrons are stored. The distance between the memory node and the island of the single electron transistor is $486nm$ which determined the sensitivity of the SET. The size of the two tunnel junctions for SET is $15\sim 25nm$ in width, $15\sim 25nm$ in length, $2nm$ in thickness, and the spacing between them is $10\sim 15nm$, i.e., the island size is $10\sim 15nm \times 15\sim 25nm$.

For the measurement of the single electron memory, the condition of the electrometer was set as the drain bias of $V_D=3V$, and the gate bias of $V_G=1.5V$ to detect the potential change of the memory node. **Fig. 10** shows the drain current of the electrometer, i.e., the single electron transistor versus the memory bias characteristics at room temperature. When the memory bias V_{MEM} of the single electron memory increases from $0V$ to $10V$, the drain current of the electrometer increases at the beginning and begins to oscillate. The drain current os-

cillation is attributed to the two effects, i.e., one is owing to the injection of the individual electrons through the multi-tunnel junction to the memory node which lowers the potential of the memory node, and the other is owing to the direct coupling of the memory bias to the island of the single electron transistor which causes the Coulomb oscillation. When the memory bias comes back from $10V$ to $0V$, the drain current follows the different trace owing to the stored electrons at the memory node and shows the clear hysteresis loop even at room temperature. The measured hysteresis loop is quite similar to that shown in Fig. 7. Owing to the large noise level in Fig. 10, however, it is difficult to distinguish the oscillation peaks owing to the electron injection to the memory node from noise peaks.

The time transient of the drain current at room temperature when the memory bias was suddenly cut off from $10V$ to $0V$ showed the step-like transient trace indicating the one by one electron ejection from the memory node to the ground. The retention time is found to be 600 seconds.

The number of electrons stored in the memory node when the memory bias of $10V$ was applied could be calculated from Eq. (2) and

$$n = \{ C_{gt} V_{MEM} - (C_{tt} + C_{gt}) V_t \} / e, \quad (3)$$

where $V_{MEM} \gg V_t$ when $V_{MEM}=10V$. Therefore, n is roughly calculated as

$$n = C_{gt} V_{MEM}/e. \quad (4)$$

Using the three dimensional simulator, the three dimensional Poisson's equation was solved for the single electron memory structure and the memory capacitance is calculated to be as $C_{gt}=4 \times 10^{-19}F$. Using this value, the number of electrons stored in the memory node is calculated to be about $n=25$.

Using the improved pulse-mode AFM nano-oxidation process, the single electron memory was fabricated on the atomically flat $\alpha-Al_2O_3$ substrate. The single electron memory stored about 25 electrons at the memory node with the applied memory bias of 10V, and showed the hysteresis loop even at room temperature. The retention time of the single electron memory is 600 seconds.

§7 Conclusions

Using the improved pulse-mode AFM nano-oxidation process, the single electron transistor and single electron memory were fabricated on the atomically flat $\alpha-Al_2O_3$ substrate. The single electron transistor shows the Coulomb oscillation with the periods of 2.1V at room temperature. The single electron memory shows the hysteresis loop even at room temperature.

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