〔RESEARCH〕

Dynamic Adaptive Devices and their Applications

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This paper introduces EHW chips currently being developed by the Evolvable Systems Laboratory at RWI center in collaboration with RWCP Adaptive Devices NEC Laboratory; a neural network EHW chip capable of autonomous reconfiguration, a data compression EHW chip for electrophotographic printers, and an adaptive control EHW chip for use in prosthetic hands and robot navigation. We also introduce latest activities at RWI center, including an analogue EHW chip for cellular phones, an EHW-based clock timing chip, and an EHW-based femto-second laser system.

§1 INTRODUCTION

In contrast to conventional hardware where the structure is irreversibly fixed in the design process, Evolvable Hardware (EHW) is designed to adapt, like the chameleon changing its color to blend in with the environment, to changes in task requirements or changes in the environment, through its ability to reconfigure its own hardware structure dynamically and autonomously. This capacity for adaptation, achieved by employing efficient search algorithms known as genetic algorithms, has great potential for the development of innovative industrial applications. The research on EHW is conducted as the development of dynamically reconfigurable adaptive devices in collaboration with RWCP Adaptive Devices NEC Laboratory.

This paper introduces five EHW chips; an analogue EHW chip for cellular phones, a neural network EHW chip capable of autonomous reconfiguration, a data compression EHW chip for electrophotographic printers, an adaptive control EHW chip for use in prosthetic hands and robot navigation, and an EHW-based clock timing chip. Finally, an EHW-based femto-second laser system is introduced, followed by the conclusion.

§2 Evolvable Hardware: Basic Concepts

Evolvable hardware is based on the idea of combining reconfigurable hardware device with genetic algorithms to execute reconfiguration autonomously2).

The structure of reconfigurable hardware devices can be changed any number of times by downloading into the device a software bit string called configuration bits. FPGA (Field Programmable Gate Array) and PLD (Programmable Logic Devices) are typical examples of reconfigurable hardware devices, for which there is already a market worth more than 2 Billion US dollars and growing at 23% per year. However it should be noted that the reconfiguration must still be executed manually by hardware designers.

A genetic algorithm (GA) is a robust search algorithm loosely based on population genetics1). It effectively seeks solutions from a vast search space at reasonable computation costs. Before a GA starts, a set of candidate solutions, represented as binary bit strings, are prepared. This set is referred to as a population, and each candidate solution within the set as a chromosome. A fitness function is also defined which represents the problem to be solved in terms of criteria to be optimized. The chromosomes then undergo a process of evaluation, selection, and reproduction. In the evaluation stage, the chromosomes are tested according to fitness function. The results of this evaluation are then used to weight the random selection of chromosome in favor of the fitter ones for the final stage of reproduction. In this final stage, a new generation of the chromosomes are "evolved" through genetic operations which attempt to pass on better characteristics to the next generation. Through this process, which can be repeated as many times as required, less fit chromosomes are gradually expelled from a population and the fitter chromosomes become more likely to emerge as the final solution.

The basic concept behind the combination of these two elements in EHW is to regard the configuration bits for reconfigurable hardware devices as chromosomes for genetic algorithms (See **Fig. 1**). If a fitness function is properly designed for a task, then the genetic algorithms can autonomouly find the best hardware configuration in terms of chromosomes (i.e. configuration bits).

For example, in data compression with EHW, we use a prediction function. Optimal prediction functions vary greatly according to the different kinds of data to be compressed. It is, therefore, not possible to design in advance a prediction hardware function. Instead of specifying a detailed hardware design, we define a fitness function. In the case of data compression, the data compression rate is used as a fitness function. Accordingly, a circuit of prediction function with a higher data compression rate is likely to remain in a population. When a good chromosome is obtained, it is immediately downloded into the reconfigurable device.

If the prediction performance of a given EHW is reduced due to changes in the nature of the data to be compressed, then the GA process is invoked and the search for a better hardware structure of prediction is initiated. In this way, EHW is capable of both autonomous and dynamic hardware reconfigurations.

The Evolvable Systems Laboratory at RWI center is collaborating with RWCP Adaptive Devices NEC Laboratory and has made three types of LSIs: a neural network EHW chip, a data compression EHW chip, and an adaptive control EHW chip. Evolvable Systems Laboratory has also developed an analogue EHW chip for cellular phones and an EHW-based clock timing chip. Below each chip is described briefly.

§3　Neural Network EHW Chip

The GRD (Genetic Reconfiguration of DSPs) chip is evolvable hardware designed for neural network applications[6]. Both the topology and the hidden layer node functions of a neural network mapped on GRD chips are dynamically reconfigured using genetic algorithms.

In neural network applications, optimal performance for a given problem is obtained by creating a neural network with the most suitable topology and the most appropriate node functions (e.g. sigmoid function or Gaussian). Furthermore, in order to meet the time constraint imposed by real-time applications, neural network hardware systems need to be 'tailored' to an ideal network size for a problem. In general, it is very difficult to design an optimal neural network and process it with scalable parallel hardware.

With GRD chip, however, the GA software on the

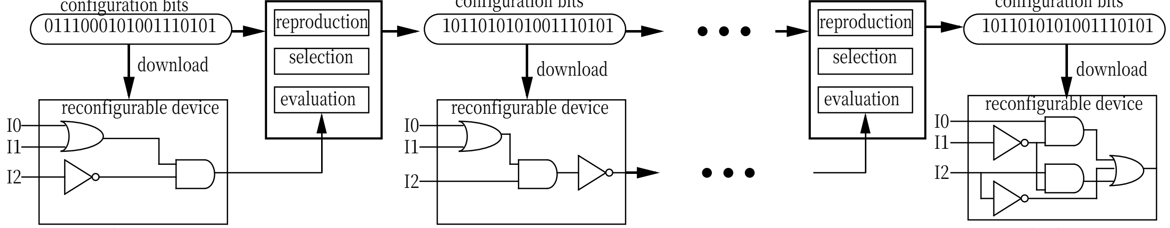

Fig.1　Basic concept of Evolvable Hardware

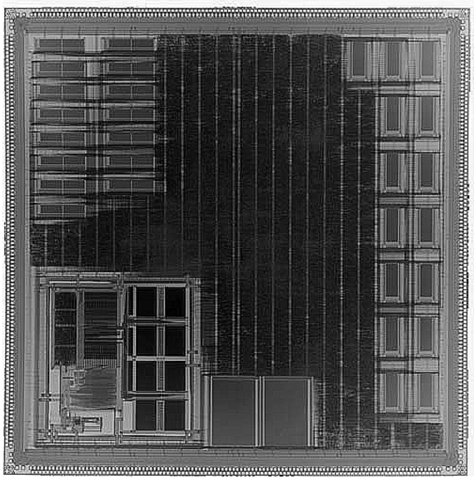

Fig.2 GRD chip

RISC processor continues to reconfigure the neural network topology and node functions in order to maintain the optimal performance.

The GRD chip consists of a 32-bit RISC processor and a binary-tree network of 15 DSPs. Each DSP can execute one node function. Using the binary-tree network, multiple GRD chips can be easily connected to configure a scalable neural network hardware.

Also, because a RISC processor is incorporated within the GRD chip, it does not need the host machine control for these tasks. This is desirable for embedded systems in practical industrial applications, together with the fast *on-line* learning capability.

The GRD chip was just manufactured in April 1998 (**Fig. 2**). The results on simulating an adaptive equalizer in digital mobile communication have showed that execution with a single GRD chip took 2.51 seconds, whereas execution on Sun Ultra2 200 MHz takes 36.87 seconds. The planned use of the GRD chip includes applications whose environments vary over time and have real-time constraints.

§4 Data Compression Chip for Electrophotographic Printing

The electrophotographic (EP) printing is the latest generation technology in the printing and publishing industry, which makes it possible to print books with a high-precision photo quality.

Data compression devices are essential for the design of EP printers, which handle large amounts of data very quickly. For example, one A4-size EP image of 1200 dpi requires 70 MBytes for storage, and EP printers processes hundreds of different pages at a speed of 100 page/min (Note that normal color copiers can print less than 10 pages/min). This means that to print a book with 100 pages, 7 giga bytes of image data must be transferred to the printer at a speed of 1800 Mbyte/min . Unfortunately, the data transfer speed of normal hard-disk drives is only 300 Mbyte/min. EP printers, therefore, have to employ data compression techniques, to (1) compress image data efficiently, and (2) to reconstruct the compressed data very quickly. However, traditional data compression techniques are insufficient both in the compression rates and decompression speeds.

The EHW data compression chip can solve these two problems by a precise prediction mechanism using reconfigurable hardware[3)]. Image data consists of values for many pixels. Because the value of each pixel tends to be closely related to its neighboring pixels, it is possible to predict the value of a given pixel based on the values of its neighboring pixels. If the value can be correctly predicted, it is not necessary to store it separately, which represents a saving in the size of the image data. This means that compression rates greatly depend on the precision of predictions. In order to increase the compression rate, it is necessary to continually reselect the most suitable prediction mechanism for the varying patterns within an image.

The prediction mechanism in the chip is implemented by EHW. Using the GA, an optimal prediction function is found and the hardware prediction mechanism is reconfigured accordingly. This leads not only to improved compression rates but also to higher decompression speed, because decompression is also carried out by the EHW hardware. The chip includes a 32-bit RISC processor hardware that executes the genetic algorithm to obtain the optimal hardware prediction.

Table 1 is the comparison with two major international

Table 1 Comparison of datacompression rate

	Printer Image	Fax Image
Lempel-Ziv	3.34	8.41
JBIG	3.35	14.67
EHW	6.52	19.82

standards for data compression; Lempel-Ziv ("compress" command of Unix) and JBIG (Joint Bi-level Image coding experts Group), both available on LSI chips. The EHW chip attained almost twice the compression rates for printer images. Arrangements have already been settled for this compression mechanism to be used in a commercial EP printer.

§5 Digital EHW Chip for Adaptive Control

This chip was developed in April 1998 to serve as an off-the-shelf device for implementing adaptive control logic[4]. Currently, this chip is applied to two applications: an autonomous mobile robot and a myoelectric artificial hand.

In most research on EHW, GAs are executed in software on personal computers or workstations. This makes it difficult to use EHW in situations that need circuits to be as small and light as possible. For example, a prosthetic hand should be of the same size as a human hand and weight less than 700 grams. Similar restrictions exist for autonomous mobile robots with EHW controllers. One answer to these problems is to integrate both the GA hardware and the reconfigurable logic into a single LSI chip.

This has been done with the digital EHW chip for adaptive control, which consists of three components, (1) PLA (Programmable Logic Array), (2) the GA (Genetic Algorithm) hardware, and (3) a 16-bit CPU core (NEC V30). Arbitrary logic circuits can be dynamically reconfigured on the PLA component according to the chromosomes obtained by the GA hardware. The CPU core interfaces with the chip's environment, as well as supporting fitness calculations when necessary. The size of the GA hardware is almost one tenth of a 32bit CPU in gate size. However, genetic operations by this chip are 62 times faster than Sun Ultra2.

Fig.3 Myoelectric prosthetic hand

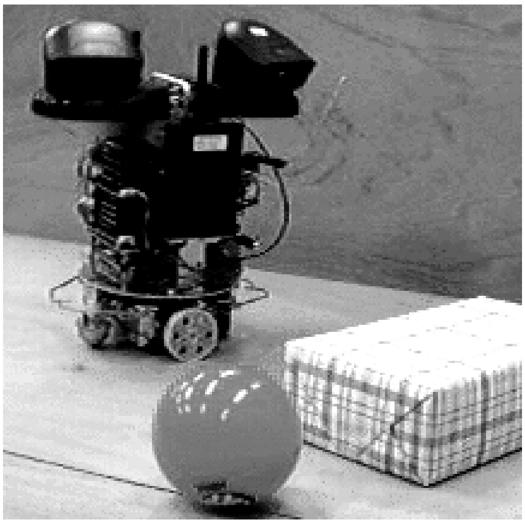

Fig.4 Autonomous mobile robot EVOLVER

The chip is being used for a control circuit in a myoelectric artificial hand (See **Fig. 3**). The hand can be controlled by myoelectric signals, which are the muscular control signals. However, myoelectric signals vary from individual person to person. Accordingly, anybody who has wanted to use a conventional myoelectric hand has to adapt to it through a long period of training (almost one month). To overcome this problem, research is carried out on controllers that can adapt themselves to the characterestics of an individual person's myoelectric signals. Most of this research is using neural networks with back propagation (BP) learning. However, learning with back propagation needs a great deal amount of time. Because the EHW chip can adapt itself quickly, the learning time can be reduced to a few minutes.

Another application is an adaptive navigation task for a real world mobile robot that must track a moving colored ball while avoiding obstacles (See **Fig.4**)[5]. Because the robot moves in an unknown and unpredictable environment, the robot is required to change its behaviour adaptively. The robot, called *Evolver*, has two camera eyes and sensors (collision and proximity), but no a-priori knowledge of the shapes and the positions of obstacles. The control logic implemented on the EHW is continuously reconfigured towards improved behaviour. For example, even if one of the sensors becomes broken, the robot autonoumously reconfigures its control logic on the EHW, within a few minutes, to continue the tracking using other functioning sensors. This adaptation speed is two orders of magnitude faster than that with classical approaches.

§6 Analogue EHW Chip for Cellular Phone

Due to the remarkable advances in recent CPUs and DSPs (Digital Signal Processors), applications with analogue circuits are rapidly being replaced with digital computing. However, there are still many applications that require high-speed analogue circuits. Communication is one such application.

However, an inherent problem in implementing analogue circuits is that the values of the manufactured analogue circuit components, such as resistors and capacitors, will often differ from the precise design specifications. Such discrepancies cause serious problems for high-end analogue circuit applications. For example, in intermidiate frequency (IF) filters, which are widely used in cellular phones, even 1% discrepancy from the center frequency is unacceptable. It is therefore necessary to carefully examine the analogue circuits, and to discard any which do not meet the specifications.

The analogue EHW chip for IF filters can correct these variations in the analogue circuits values by genetic algorithms[10]. Using this chip provides us with two advantages.

The first is an improved yield rate. When an analogue EHW chips are shipped, which do not satisfy specifications, then the GA can be executed to alter the defective analogue circuit components in line with specifications. The GA is supposed to be executed in the LSI tester.

The second is smaller circuits. One way to increase the precision of component values in analogue LSIs has been to use large valued analogue components. However, this involves larger circuits, and accordingly higher manufacturing costs and greater power consumption. With the EHW chip, however, the size of the analogue circuits can be made smaller. Obviously, smaller IF filters are particularly welcome in cellular phones, but similar considerations exist in a wide variety of applications where analogue circuits are used.

Figrue 5 illustrates the analogue EHW chip. The chip includes 39 G_m components (transconductance amplifiers) whose values can be set genetically. The values, which actually control the base current of the CMOS, are coded as configuration bits. Each G_m element value may differ from the target value up to a maximum of 20%. All of the 30 chips manufactured for the experiment could be corrected to satisfy the IF filter's specifications. The chip was manufactured in Spetember 1998.

§7 An EHW-based Clock Timing Adjusting Chip

The demand for high-speed LSIs, such as Pentium III(500 MHz) and DEC Alpha (600MHz), is increasing. Unfortunately, the yield rates for such fast digital systems are rather poor. Typically, in the early stages of mass production, yield rates are less than 10%. One of the reasons for the poor yield rates is that the timing delays between digital components often do not conform to the design specifications. Such discrepancies arise

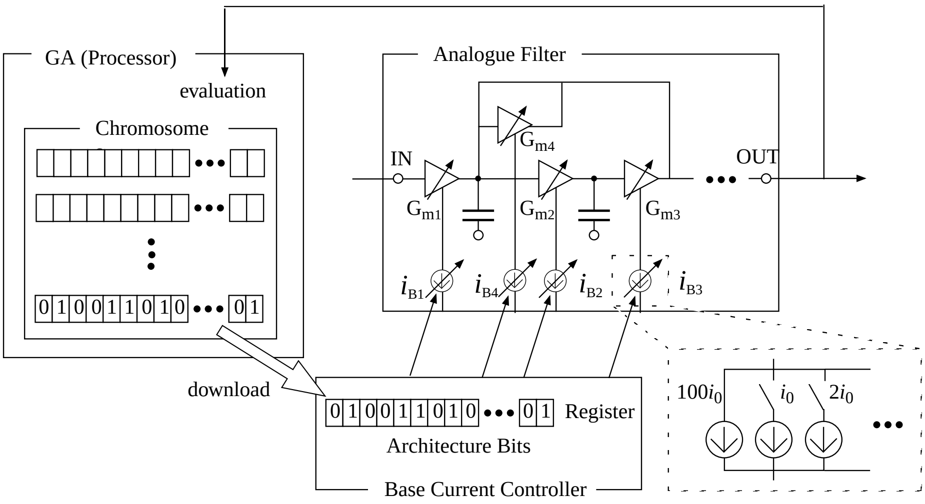

Fig.5 Basic idea of the analogue EHW chip for IF filters

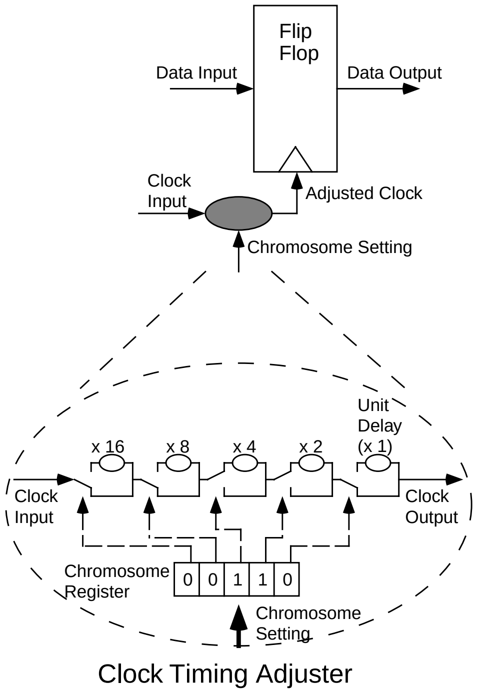

Fig.6 Clock-timing Adjuster

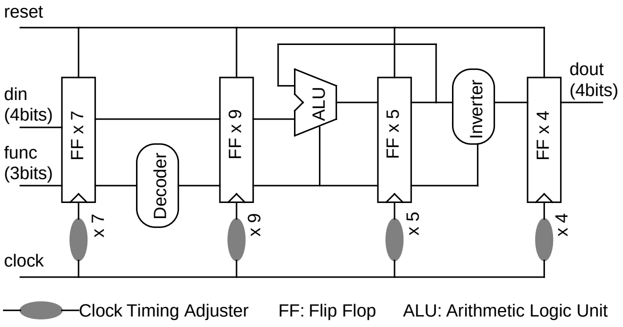

Fig.7 Evolvable Memory Test Pattern Generator

from variations in the values of parasitic capacitances and resistors along the data lines between digital components, which can differ significantly depending on the LSI. Variations in clock timing are referred to as "clock skew." LSIs that fail to satisfy design specifications because of clock skew are simply discarded, leading to poor yield rates.

In order to solve this problem, we propose an EHW-based clock-timing adjusting architecture for high-speed digital systems9). Instead of simply discarding chips that do not meet the specifications, we can genetically adjust the clock timings in the LSI in order to conform to the specifications(**Fig. 6**).

We have developed a LSI, which is used in the high-speed memory tester, to show the advantages of this architecture(**Fig. 7**). Simulation results show that the number of LSIs that can operate at 800 MHz increases from 2.9% to 51.1% after the clock-timing circuits have been evolved by the GA. This clock-timing adjusting architecture is, therefore, expected to become a basic LSI technology for GigaHz digital systems.

§8 An EHW-based Femto-second Laser System

Laser systems must be aligned precisely, because the

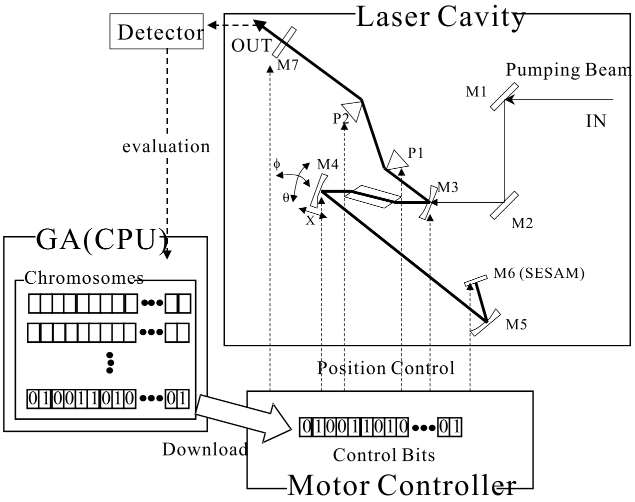

Fig.8 Evolvable Memory Test Pattern Generator

light has to travel many times within a laser cavity before returning to the focus point with μm resolution. This is particularly true of the high-peak power involved in femtosecond pulse lasers, which the distorting nonlinear lens effects should also be considered. It, therefore, typically takes about a week to manually align a femtosecond laser, where the optimal condition must be determined empirically. In order to overcome this problem, we propose and demonstrate an evolvable laser system that can adjust the positioning of the laser cavity components (e.g. the mirrors and prisms) by genetic algorithms, which incorporate a special local learning method. In an initial experiment, an output power was obtained which is 2.3 times higher than the power achieved with a manual alignment set in our laboratory. This laser system has three advantages, namely; (1) higher output power, (2) automatic and reliable adjustment and (3) compactness, all of which are important prerequisites for femtosecond laser technologies to become a widely-used industrial technology. The overview of the laser system is shown in **Fig. 8**.

§9 CONCLUSION

In this paper, five LSIs are introduced as application examples of dynamically adaptive devices. Although their usefulness is obvious, we need to show more examples of industrial applications. Besides these LSIs, RWI center is working for the developments of an evolvable femto-second laser systems, evolvable microwave circuits, self-repairing FPGAs and so on. In self-reapiring FPGAs, we plan to integrate statically adaptive devices with dynamically adaptive devices.

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