

§4 Feasibility-Study of FRDC Method

4. 1 Introduction

The accuracy of the thermal ac-dc transfer standards is determined by the uncertainty in the evaluation of thermoelectric transfer difference which is caused by the non-joule heating due to the Thomson and the Peltier effect. A fast-reversed dc (FRDC) source has been developed at PTB for the evaluation of the thermoelectric transfer difference. However, the technical difficulties in the original FRDC source prevented the realization of the uncertainty in the evaluation at 0.1 ppm level, as will be described in the section 4.2.

A new modified FRDC waveform was proposed in order to overcome the difficulties and improve the accuracy of the FRDC method. The new FRDC sources, which are based on the modified waveform, have been developed at ETL during the years 1992 to 1994. The development at ETL may be divided to the following three stages.

- [1] The ‘first-stage’ circuit to examine the feasibility of the modified FRDC waveform.
- [2] The ‘second-stage’ evaluation circuit based on the new switching scheme to reduce the ‘memory-effect’ of analog switches.
- [3] The ‘production-model’ FRDC source designed for the small-scale mass-production.

In this chapter, development of the first- and the second-stage evaluation circuits are described. The evaluation circuits were developed for the purpose of examining the feasibility of the FRDC method as the basic reference in the ac-dc transfer standards. The technical difficulties mentioned above have successfully been overcome in the course of the feasibility study, as will be described in detail in the following sections. The ‘production model’ FRDC source developed in the third-stage will be described in the next chapter (§5).

4. 2 Original and modified waveform

4. 2. 1 Effect of imperfect switching

In the case of original FRDC source developed at PTB, the rectangular-waveform ac voltage has been synthesized by reversing the polarity of dc source using high-speed analog switches[25]. The FRDC-DC difference of a thermal converter is measured using the FRDC mode and the two dc (DC+, DC-) modes. In order to obtain the equality between the RMS of the FRDC and the mean of the two dc modes, perfectness of the switching is required. More specifically, the following two sources of error must be negligible at the required level of precision.

(1) Slew rate of analog switches

The sharpness of the rising- and falling-edge of the FRDC waveform is determined by the slew rate of the analog switches. If the rise and the fall of the edges take 10 ns, the rms power of the order of 10^{-8} may be lost at every switching. Assuming that the output voltage changes linearly at the rising- and falling-edges during the switch-over period Δt_{sw} , The power-loss ΔP_{sw} due to the slew rate is calculated as

$$\frac{\Delta P_{sw}}{P_0} \approx \frac{2\Delta t_{sw}}{3T_{sw}} = \frac{2}{3} \Delta t_{sw} f_{sw}. \quad (4.1)$$

Here the parameters T_{sw} , f_{sw} and P_0 represent the switching period, switching frequency, and total power of the FRDC waveform, respectively. The loss of the rms value increases proportionally with the switching frequency. At the switching frequency of 100 Hz, the relative loss of the rms power for the switching period of 10 ns is calculated as 6.7×10^{-7} .

(2) Effect of transients

The transients such as overshoot or ringing at the time of the switching also directly affects the rms value. In the actual circuit conditions, it is very difficult to suppress the transients. Hence in most of the cases, the effect of the transient is larger than the effect from the slew rate. As in the case of the slew rate, the change in the rms value due to the transients is proportional to the switching frequency.

The effect from the slew-rate and transients may be corrected by measuring the actual waveform by a high-speed oscilloscope. However, it is very difficult to achieve the accuracy of the correction better than 10^{-7} owing to the limited accuracy in the measurement of high-speed voltage measurement. A more practical approach is to use the assumption that the effect from the slew-rate and transients are proportional to the switching frequency. In this case, the extrapolation of the FRDC-DC difference value to 0 Hz should give the value without the effect from the slew-rate or transients.

In addition to the requirement for the perfectness of the switching, there is also a strict requirement on the output-level of the FRDC waveform. Since the FRDC mode is produced by switching between the two dc levels (DC+, DC-), the output levels in the FRDC mode are assumed to be equal to the levels in the dc modes. This assumption does not necessarily hold at the precision of 0.1 ppm level, and it is very difficult to evaluate the equality of the dc-levels. This is a critical problem when the method is used as a basis of the ac-dc transfer standard.

4. 2. 2 Effect of high-frequency harmonics

The rectangular waveform of the FRDC mode contains a large number of high-frequency harmonics. The power in the high-frequency harmonics may be reduced or enhanced due to the frequency response of the TC-input circuit. In this section, the error in the rms value is evaluated for a simple case in which the frequency response of the input circuit can be approximated by a first-order low-pass filter.

The power of the $(2n-1)$ th harmonics P_{2n-1} of the FRDC waveform decreases as

$$P_{2n-1} / P_0 = (2/(2n-1)\pi)^2. \quad (4.2)$$

For example, a FRDC waveform with switching frequency $f_{sw}=200$ Hz has the basic frequency $f_0=100$ Hz, and the 1001st harmonic at 100.1 kHz contributes 0.4 ppm of the total power.

The decrease of rms power of $(2n-1)$ th component by the low-pass filter with cut-off frequency f_c is approximately given by

$$\Delta P_{2n-1} / P_{2n-1} = (2\pi(2n-1)f_0/f_c)^2. \quad (4.3)$$

In the case of the low-pass filter of 1 GHz cut-off frequency, the decrease of rms power at 100 kHz is 0.04 ppm. As illustrated in **figure 4.1**, the power of the n -th harmonic is proportional to $1/n^2$ while the decrease of rms power by the low-pass filter is proportional to n^2 . As a result, the loss of rms power for each harmonic becomes independent to n :

$$\Delta P_{2n-1} / P_0 = (4f_0/f_c)^2. \quad (4.4)$$

Assuming that harmonics in the output waveform are uniformly distributed up to the cut-off frequency, the accumulated loss in the rms power is approximately given as

$$\sum_{n=1}^{f_c/f_0} \Delta P_{2n-1} / P_0 \approx (4f_0/f_c)^2 \times (f_c/2f_0) = 8f_0/f_c. \quad (4.5)$$

Thus the accumulated loss in the rms power is proportional to the switching frequency. In the case of a FRDC

waveform with $f_0=100$ Hz being applied to the 1 GHz low-pass filter, the decrease of rms power for each harmonics is as small as 1.6×10^{-14} with respect to the total power. However, the accumulated loss in the rms power becomes of the order of 0.8 ppm. Thus even when the basic frequency is 7 decade smaller than the cut-off frequency, the FRDC-DC difference measurement is affected at 1 ppm level. This is the fundamental difficulty of the FRDC method which has been pointed out since the early stage of research at PTB.

4. 2. 3 Modified waveform

To overcome the problem of the slew rate and the transient of the original FRDC waveform, the authors have proposed a modified FRDC waveform [27]. The original and the modified FRDC waveforms are illustrated in **figure 4.2**. In the modified waveform, the switching is performed not only during the FRDC-mode but also during the dc-modes. In this case, the dc-waveform is no-longer the steady-state dc. The switching is performed between “+” output-level and “off” (zero) output level in the case of DC+ mode. In the DC- mode, the switching is performed between “-” out-

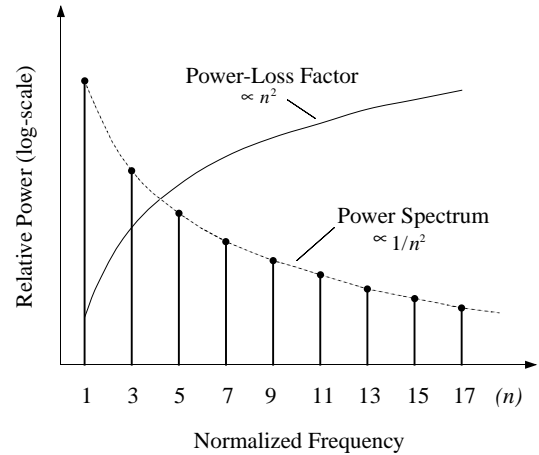


Figure 4.1 Effect of higher-order harmonics of FRDC waveform. The power of the n -th order component of FRDC waveform decreases as $1/n^2$, while the decrease of rms power by a low-pass filter is proportional to n^2 . Hence the effect of higher-order component does not decrease with frequency.

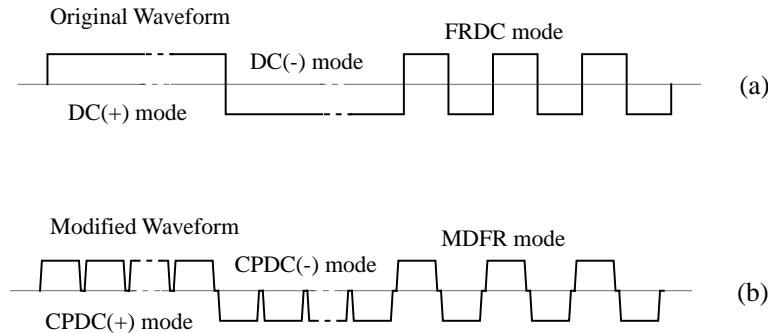


Figure 4.2 (a) Original waveform with DC+, DC- and FRDC modes. (b) Modified waveform with two ‘chopped’ dc (CPDC) modes and a modified fast-reversed dc (MDFR) mode.

put-level and “off” (zero) output level. We hereafter call the modified dc modes as “chopped dc” (CPDC) modes. Similarly, in the modified FRDC mode (MDFR mode), the switching is performed between “+” output-level, “-” output-level and “off” (zero) output level with exactly same timing as in the case of CPDC modes. In the modified waveform the “off” states are equally distributed in the CPDC-modes and the MDFR-modes.

An important constraint on the off-time is that the duration of the off-time t_{off} should be sufficiently smaller than the thermal time-constant τ of the thermal converter.

$$t_{off} \ll \tau \quad (4.6)$$

When this constraint is satisfied, the temperature distribution along the heater of TC equals to that for the steady-state dc. From the thermal point of view, the CPDC modes may be regarded as equivalent to the steady-state dc modes when the condition (4.6) is satisfied.

As shown in the figure, the MDFR waveform may be recognized as a combination of one cycle of CPDC+ waveform and one cycle of CPDC- waveform appearing alternately. The rising-edges and the falling edges in the CPDC waveform are reproduced in the MDFR modes. Since the effects of slew-rate and transients are compensated between the CPDC- and the MDFR-modes, the equality of the rms-values for the two modes is realized with only moderate requirements for the response-time of the circuit. In order to obtain the same rising-edges and the falling edges in the MDFR- and CPDC-waveform, the edges must be separated longer than the transient period of the switching. Hence another important constraint on the off-time is that the duration of the off-time t_{off} should be sufficiently longer than the transient-time Δt_{sw} of the analog switches.

$$t_{off} \gg \Delta t_{sw} \quad (4.7)$$

The off-time t_{off} is usually set to 10 μ s which satisfies the two requirements (4.6) and (4.7).

In the modified waveform, not only the MDFR waveform but also the CPDC waveforms have high-frequency components due to periodical glitches. Since the numbers of rising edges and falling edges are same for the MDFR- and the CPDC waveforms, the two waveforms have similar distribution of high-frequency harmonics. As a result, the effect of high-frequency harmonics compensates each other between the MDFR- and the CPDC-modes. This is an important by-product of the modified waveform, and will be treated in detail in section 6.3.

In the case of the original waveform, the rms voltage of the FRDC waveform is determined by the well defined two dc levels. Hence it is possible to use the FRDC waveform as a precise ac voltage reference. In the case of modified waveforms, neither the MDFR nor the CPDC waveform has the

well-defined rms value. However, the equality of the rms power between the two modes is the only requirement for the precise evaluation of thermoelectric effects in the thermal converters.

4.3 First-stage evaluation circuit

4.3.1 Circuit description

The first evaluation circuit has been developed in 1992, for the purpose of examining the effectiveness of the modified FRDC waveform. The schematic circuit diagram of the FRDC circuit is shown in **figure 4.3**. Since the effects from the slew-rate and the transients are compensated in the modified waveform, only moderate performance for the frequency characteristic of the circuit is required. For this reason, general-purpose analog-switch (AD7510) has been used as the switching element. As the typical ON/OFF switching time of the AD7510 are 180/350 ns respectively, the off-time of 10 μ s should be sufficient to satisfy the condition (4.7).

The analog switches have relatively large “on”-resistance (75 Ω for AD7510), which is not negligible compared with the input resistance of TVCs (25 Ω - 1 k Ω). Hence the output of the FRDC circuit was designed as a constant-current output. Since the ON-switching-time of the AD7510 is shorter than the OFF-switching time, it is suitable for the ‘make-before-break’ operation required for the switching of the current-output.

The schematic diagram of FRDC-DC difference measurement circuit is shown in **figure 4.4**. The ON-OFF sequence of the analog switch was controlled by the programmable pulse generator-circuit. The pulse generator and the main FRDC circuit are electrically isolated using opto-couplers. The EMF-output of the test-TC is directly measured by a nano-voltmeter (Keithley K182).

4.3.2 Results

The thermoelectric transfer differences of two SJTC elements were evaluated by the FRDC-DC difference measurement using the first evaluation circuit. Measurement sequence

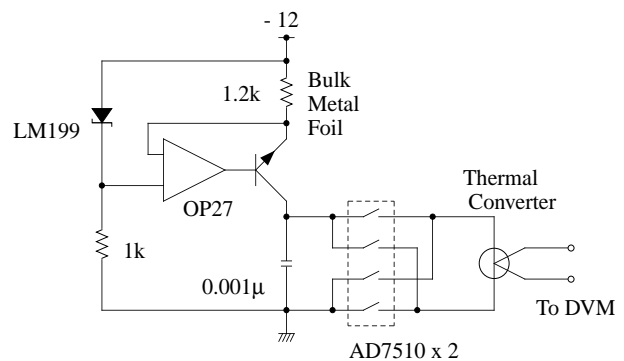


Figure 4.3 The circuit diagram of the first-stage evaluation circuit. Switching elements are CMOS analog switches (AD7510) with typical on (off) time of 180 (350) ns. The output circuit was designed as a constant-current source.

[FRDC, DC+, DC-, FRDC] has been used for the FRDC-DC difference measurement in order to compensate the linear drift in the output of SJTC-elements. As in the case of the comparator system, the detection sensitivity is mainly determined by the resolution of the K182 nanovoltmeter. Taking the average of 100 readings, resolution of 0.1 ppm in the FRDC-DC difference has been obtained.

An example of the results from the FRDC-DC difference measurement is shown in **figure 4.5**. The measurement was performed at switching frequencies from 111 Hz to 500 Hz. The TC element specified as TC91-T03 in the figure is a type-SS283 SJTC element used in the standard TVCs of ETL. The other TC-element specified as TC105921 is one of the original ETL-design SJTC used in the former standard [36]. Both of the SJTCs were measured at 6 mA, i.e., at 60% of the rated current. As shown in the figure, the measured FRDC-DC differences show small linear dependencies to the switching frequency. The linear dependence implies that some residual error is added at every switching.

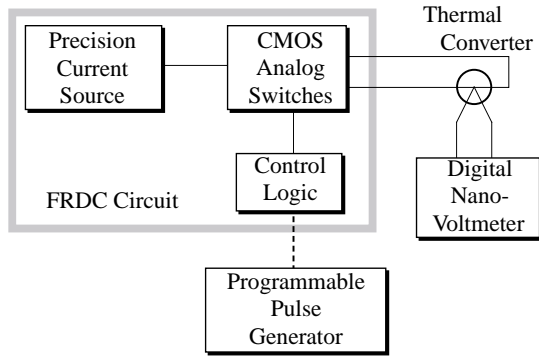


Figure 4.4 The schematic diagram for a FRDC-DC difference measurement. The programmable pulse generator produces the timing for the on-off operation of the analog switches. The EMF-output of the thermal converter is measured by a nano-voltmeter.

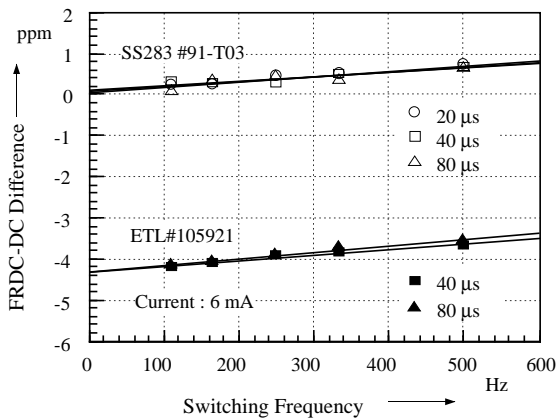


Figure 4.5 Results of the FRDC-DC difference measurement on SJTCs using the first evaluation circuit. The SJTC specified as #91-T03 in the figure belongs to the new standards of ETL. The other SJTC specified as ETL#105921 belongs to the former ETL standard.

Hence the extrapolations to 0 Hz were used in estimating the thermoelectric transfer difference of the SJTCs.

The thermoelectric transfer differences of the two SJTCs were also evaluated by using the MJTC from PTB (PTB#73) as a reference standard. The comparisons of the ac-dc difference were performed at 1 kHz, 6 mA, using the ac-dc comparator described in chapter 3. As shown in **table 4.1**, the values of thermal transfer difference evaluated by the two methods agreed to 0.1-ppm level for both TC#91-T03 and ETL#105921.

The MJTC from PTB is one of the most reliable reference in the ac-dc transfer standard, and its thermoelectric transfer difference is theoretically evaluated to be smaller than 10^{-7} [13]. The agreement of 0.1 ppm-level with the MJTC indicates the effectiveness of the FRDC method for the evaluation of the thermoelectric transfer difference. Furthermore, the agreement of the two independent methods of evaluation, i.e., the theoretical evaluation in MJTC and experimental evaluation in the FRDC method, gives us a confidence in the reliability of the present ac-dc transfer standards.

On the other hand, the linear dependence of the FRDC-DC difference with the switching frequency implies the existence of some unknown source of error. The resolution of this phenomenon was one of the main goal in the development of the second-stage evaluation circuit.

4. 4 Source A/B-switching scheme

4. 4. 1 Memory-effect

As described in the previous section, a linear dependence of the FRDC-DC difference with the switching frequency is observed in the case of first evaluation circuit. The positive slope of the frequency dependence suggested that small amount of power is lost at every reversal of the polarity.

One possible cause which may account for the loss of power is the charge-trapping effect at the analog switches. In this case, the loss of power are caused by the following procedures;

- [1] When the FET-channels of the analog switches make transition from low-resistance (ON) state to high-resistance (OFF) state, some charges are trapped in-

Table 4.1 The thermoelectric transfer difference of SJTCs #91-T03 and ETL#105921 evaluated by the FRDC method. The two SJTCs were also evaluated by comparison to the MJTC from PTB (PTB#73).

T.C. Unit	Estimated by FR-DC Method	Comparison to MJTC(PTB#73)
Model SS283 #91-T03	0.07 ± 0.12	-0.03 ± 0.12
Model ETL #105921	-4.33 ± 0.15	-4.56 ± 0.11
in ppm		

- side the channel due to channel-to-ground capacitance.
- [2] In the next reverse transition from the OFF state to the ON state, the trapped charges are imposed on the output current.
 - [3] In the FRDC mode, the polarity of the output current changes at switching, and the trapped charges tend to reduce the output current during the transition. While in the CPDC mode, the polarity is kept constant and the reduction of the current does not occur.

Owing to the charge-trapping effect, the small portion of rms power is lost at every reversal of the polarity in FRDC mode, giving rise to a positive slope in the FRDC-DC difference. We hereafter call this effect a “memory-effect” of the analog switches. Using the typical value of channel to ground capacitance of 8 pF and the potential (0.5 V) of the channel for the “on” state of the analog switch, the amount of the trapped charge is estimated to be of the order of 4 pC. If all the trapped charge is emitted to the output circuit from the four gates, the memory effect can cause the frequency dependence of 3 ppm/kHz, which is in good agreement with the measured frequency dependence.

4. 4. 2 New switching scheme

According to the consideration described above, a new switching scheme has been introduced in the second evaluation circuit[28], for the purpose of reducing the ‘memory-effect’. The principle of the new switching scheme is illustrated in **figure 4.6**. In the new scheme, the waveforms are divided into the two periods, i.e., ‘Phase-A’ and ‘Phase-B’. During the phase A, output is supplied from the source A, and the output from the source B is isolated from the TC. During the phase B, TC is connected to the source B and isolated from the source A. Shortly before the transition from

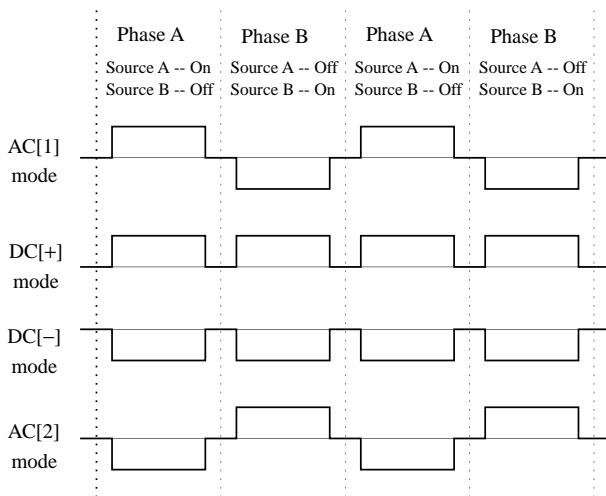


Figure 4.6 The principle of the new switching scheme. The waveform is synthesized from the two intervals, ‘Phase A’ and ‘Phase B’. In the new scheme, switching between the source A and the source B is always performed at zero output-level in order to suppress the ‘memory effect’ of the analog switches.

the phase A to the phase B, the source A switches from on-state to off-state. After transients die out, TC is disconnected from the source A and is connected to the source B. Then the source B switches from off-state to on-state. By the combination of the output-polarities of the sources A and B, the two ‘modified’ FRDC modes [MDFR(1), MDFR(2)] and the two ‘chopped’ dc modes [CPDC(+), CPDC(-)] are obtained.

In the new scheme, switching between the source A and the source B is always performed at zero output-level (off-state). Consequently, it should be possible to suppress the memory-effect due to the analog switches.

4. 4. 3 Equality of the rms values

The schematic diagram of the circuit based on the new switching scheme is shown in **figure 4.7**. In the new circuit, the output is supplied alternately from the two independent bipolar current sources (A and B), and the two critical switches at the output operate only at the zero voltage states.

A FRDC-DC difference for the new source is obtained in a similar way as the original definition (1.8). The EMF for the FRDC mode is defined as the mean of the EMFs for the two MDFR modes. The equality of the rms values of the two MDFR modes and the two CPDC modes are expressed as,

$$\begin{aligned} \langle i_{MDFR(1)}(t) \rangle_{rms}^2 + \langle i_{MDFR(2)}(t) \rangle_{rms}^2 \\ = \langle i_{CPDC(+)}(t) \rangle_{rms}^2 + \langle i_{CPDC(-)}(t) \rangle_{rms}^2. \end{aligned} \quad (4.8)$$

Though it is not difficult to realize the equality (4.8) at 0.1 ppm level, it is not easy to evaluate or prove the equality at the same level of precision. This has been a fundamental drawback of the first evaluation circuit. In the case of the new circuit, the equality is satisfied on condition that there is no correlation between the outputs of the two sources, and

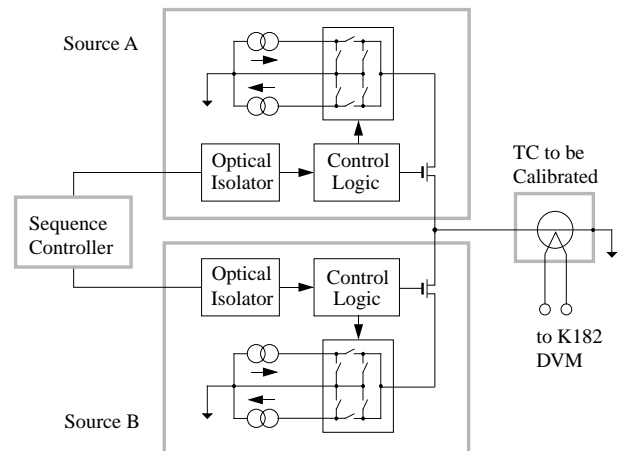


Figure 4.7 The schematic diagram of the new FRDC circuit. The output is supplied alternately from the two independent bipolar current sources (A and B). By the combination of the output-polarity of sources A and B, the two MDFR modes and the two CPDC modes are obtained.

the following four conditions are satisfied.

- The source A outputs exactly the same waveform for the MDFR[1] mode and CPDC[+] mode.
- The source A outputs exactly the same waveform for the MDFR[2] mode and CPDC[-] mode.
- The source B outputs exactly the same waveform for the MDFR[1] mode and CPDC[-] mode.
- The source B outputs exactly the same waveform for the MDFR[2] mode and CPDC[+] mode.

In other words, the waveform from the sources A/B should not be affected by the polarity of the output of the other source. It is also possible to check the above four conditions experimentally, as will be described in detail in section 5.4.4. The new switching scheme has realized the quantitative evaluation of the uncertainty in the equality of rms value between the FRDC modes and the dc modes. This feature is another major advantage of the new switching scheme.

4.5 Second-stage evaluation circuit

4.5.1 Circuit description

A new version of the FRDC source was developed in 1993, for the purpose of evaluating the effectiveness of the new switching scheme. In order to avoid the possible interference between the two sources, the new FRDC source was developed with the following design-criteria;

- The sources A and B have mutually isolated power supplies.
- The control-lines to the sources A and B are electrically isolated using optical isolators.
- The circuits of the sources A and B are separately shielded to avoid both thermal and electromagnetic couplings .

The analog part of the second evaluation circuit has been developed at ETL. The schematic diagram of the circuit is shown in **figure 4.8**. Only one of the two sources (source A or source B) is shown in the figure. The circuit consists of a high-stability bipolar current source and three high-speed analog switches. The circuit, combined with the other half, generates the two MDFR waveforms and the two CPDC waveforms according to the status- and the timing-signals from the ‘Sequence Controller’. Two D-type latches and two NAND gates receive the status signal ‘ON/OFF’ and timing-signal ‘SYN’ from the Sequence Controller and create the switching sequence for the analog switches. Selection of the four modes is controlled by the ‘MODE’ signal from the Sequence Controller. The positive and the negative outputs from the current sources are connected to either the load(output) or to the dummy resistor by the analog switch according to the ‘MODE’ status. In the second evaluation circuit, switching elements are changed to high-speed CMOS analog switches (IH5143) which have typical on(off)-time of 80 (50) ns.

Another advantage of the new circuit is that it is possible to define the fixed ground for TC-input by con-

necting the ‘Signal-Lo’ of TC-input to the ground. This configuration is required for the measurements on MJTCs which is sensitive to electrostatic breakdown. In the case of the first evaluation circuit, the TC-input circuit was exchanged at each switching, and it was not possible to define the fixed ground.

The digital part of the second evaluation circuit was developed at JEMIC. The schematic diagram of the circuit is shown in **figure 4.9**. The digital circuit is controlled by a

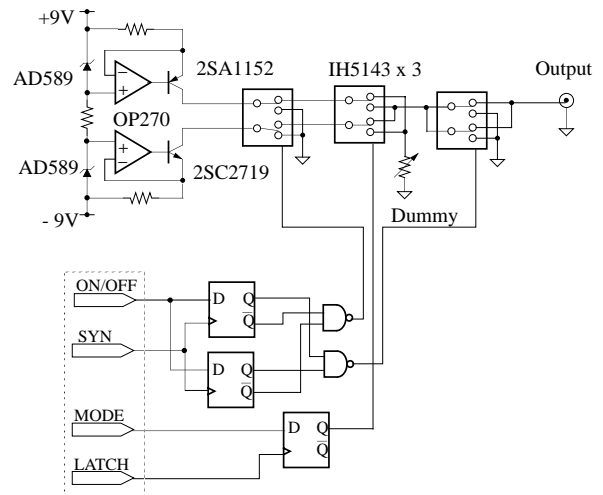


Figure 4.8 The schematic diagram of the analog part of the second evaluation circuit (source A or source B). The switching sequence of the analog switches is controlled by the status signal ‘ON/OFF’ and timing-signal ‘SYN’ from the Sequence Controller. Selection of the four modes (two MDFR- and two CPDC-modes) is controlled by the ‘MODE’ and ‘LATCH’ signal.

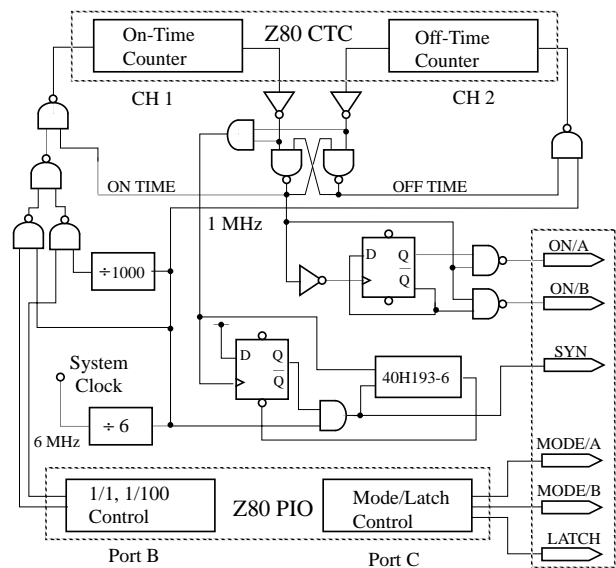


Figure 4.9 The schematic diagram of the digital part of the second evaluation circuit. The circuit is controlled by a Z84C011 micro-processor. The status signal ‘ON/OFF’ and timing-signal ‘SYN’ control the switching sequence of the analog switches. The ‘MODE’ signal selects one of the four output-modes.

Z84C011 micro-processor which includes an Z80 CPU, programmable I/O ports (PIOs), and Programmable Timer/Counters (CTCs). The CTCs and HC-MOS logic circuit produce the status signal 'ON/OFF' and timing-signal 'SYN'. These signals control the switching timing of the analog switches in the analog circuit. The 'MODE' signal is generated at the PIO-port C. The micro-processor is operated by a program written in an EPROM. A GP-IB interface board connects the micro-processor to the system-controller.

4.5.2 Results

Both the digital part and the analog part of the second-stage evaluation circuit were completed in February 1993. The two parts were brought to PTB and were combined with high-isolation power supplies made by PTB. Then a collaborative research has been performed for a period of three month. The performance of the FRDC circuit was evaluated at PTB using different types of SJTCs, and MJTCs.

(1) MJTC (PTB#88) from PTB

The result of the evaluation using the MJTC (PTB#88) is shown in **figure 4.10**. Here, the FRDC-DC difference of the MJTC was measured at the currents of 6 mA and 10 mA. The measurement was performed for the frequency range of 10 Hz to 10 kHz with the off-time set to 10 μ s. The experimentally determined thermoelectric transfer difference from the FRDC-DC difference measurement is -0.05 ± 0.1 ppm at 10 mA, in good agreement with the theoretical estimation [13].

One of the main goals of the second evaluation circuit was the reduction of the linear frequency dependence due to the memory effect. As shown in the figure, the frequency dependence of the FRDC-DC difference was reduced to be less than 0.3 ppm up to 10 kHz, which confirms the effectiveness of the new switching scheme employed in the sec-

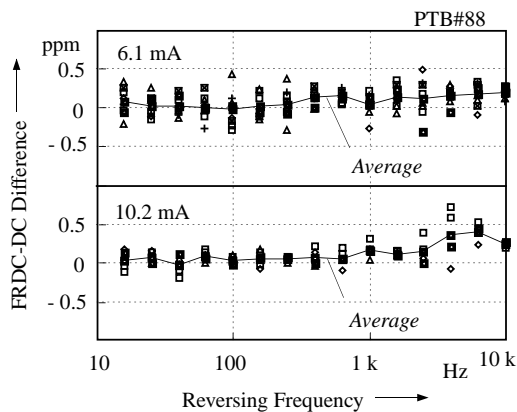


Figure 4.10 Result of FRDC-DC difference measurement of the MJTC (PTB#88) from PTB. The measurement was performed at the current of 6 mA and 10 mA with 10 μ s off-time. By the use of the new switching scheme, the linear dependence on the switching frequency was reduced to be less than 0.3 ppm up to 10 kHz.

ond evaluation circuit.

(2) MJTC from Guildline (GL#32472)

The result of FRDC-DC difference measurement for the MJTC from Guildline (GL#32472) at 10 mA is shown in **figure 4.11**. As shown in the figure, the measured FRDC-DC difference was found to be dependent on the resistance of the 'dummy' resistors in the source A/B circuit. In this case, mismatching as small as 10 % may affect the measurement at 0.1 ppm level. As will be described in section 5.4.2, the effect was traced to the drift in the bias current of the output transistor of source A/B circuit. After replacing the transistors with FETs, this phenomenon was reduced below the detection sensitivity.

When the MJTC (GL#32472) is used at voltage mode, and is calibrated against a MJTC from PTB, the MJTC shows fairly large ac-dc difference of the order of -2 ppm at 1 kHz. On the other hand, from the result of the FRDC-DC difference measurement, the thermoelectric transfer difference at current mode is evaluated to be less than the detection sensitivity (<0.3 ppm). In order to investigate the cause of this discrepancy, the calibration of MJTC (SN#32472) at current mode was carried out using the MJTC from PTB as a reference. The ac-dc difference of MJTC (SN#32472) in the current mode was found out to be smaller than 0.5 ppm, in good agreement with the FRDC-DC difference measurement. The existence of such large difference in the thermoelectric transfer difference of MJTCs was not known before. This is an important by-product obtained in the course of the development of the second evaluation circuit.

(3) SJTC from Best Product (#S10-29)

The measurements of the thermoelectric transfer differences of a SJTC (#S10-29) were performed at the reversing frequencies between 0.1 Hz to 10 kHz. The SJTC is an old model from Best Product with nominal current of 10 mA.

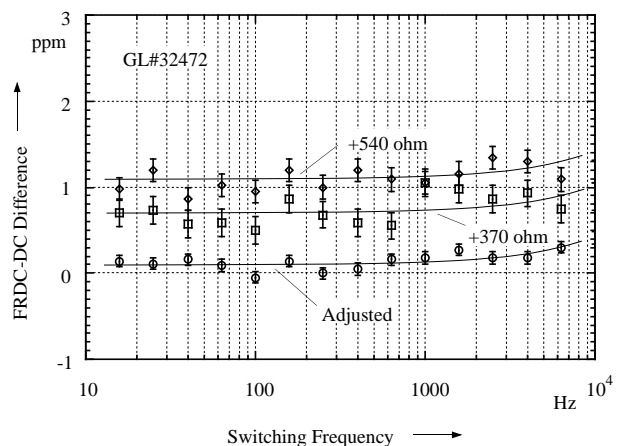


Figure 4.11 The result of FRDC-DC difference measurement for the MJTC from Guildline (GL#32472) at 10 mA. The measured FRDC-DC difference was dependent on the resistance of the 'dummy' resistors.

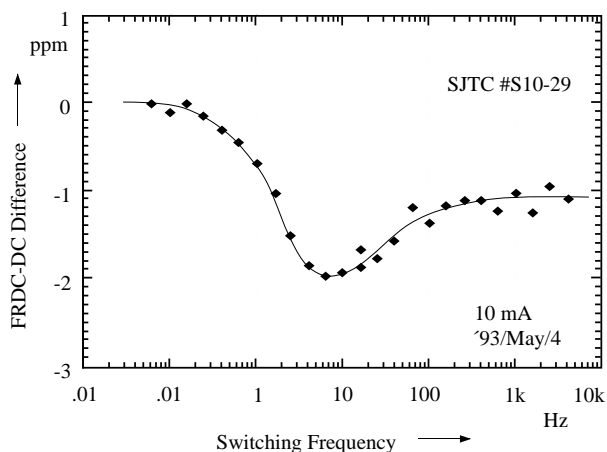


Figure 4.12 Result of FRDC-DC difference measurements for a SJTC (#S10-29). The FRDC-DC difference shows a complicated frequency characteristic which may be explained by a combination of two kinds of thermoelectric effects with opposite polarity and with different characteristic time constants.

The result of the measurement is shown in **figure 4.12**. As shown in the figure, the FRDC-DC difference of the SJTC shows a complicated frequency characteristic. This phenomenon may be explained by a combination of two kinds of thermoelectric effects with opposite polarity and with different characteristic time constants. It is the first successful demonstration on the effectiveness of the FRDC method as a basic tool for investigating thermoelectric effects in TCs. The relation of the characteristic time constant of the thermoelectric effects and the frequency dependence of the FRDC-DC difference of a TC is described in detail in the chapters 6 to 7.

4.6 Summary

By the use of the improved waveform employed in the first and the second evaluation FRDC circuit, it was possible to overcome the difficulty of the original FRDC method caused by imperfect switching of the analog switches and effect of higher frequency component of the rectangular waveform. In addition, the new switching scheme employed in the second evaluation circuit solved the problem of the 'memory effect', and provided an experimental procedure to evaluate the equality in rms value between the FRDC and the dc modes.

The FRDC measurement using either the first or the second evaluation circuit has yielded the good agreement with the MJTC from PTB at 0.1 ppm level. The thermoelectric transfer difference of the MJTC was evaluated theoretically using mathematical modeling, while in the case of the FRDC method, the thermoelectric transfer differences are determined experimentally. The good agreement between those two methods indicates the reliability of both methods as a basic reference in the ac-dc transfer standards.