

## §5 Development of a FRDC Source

### 5.1 Introduction

The feasibility-study on the modified FRDC waveform has been performed on the first- and the second-stage evaluation circuits, as described in chapter 4. The usefulness of the FRDC source for determining the thermoelectric effects in thermal converters have been confirmed through the development of these evaluation circuits. Then, we started to develop a 'production-model' FRDC source as the final stage in the development of the FRDC source based on the modified waveform. The production-model FRDC source was developed as a cooperative research project between PTB, CSIRO/NML, JEMIC and ETL. In this chapter, detailed design and the result of evaluation of the production-model FRDC source are described in detail.

### 5.2 Development of the production model

The development of the 'production-model' FRDC source has been started in May 1993, following the evaluation of the second evaluation-model FRDC circuit at PTB. The production model [59] was named "KST003 FRDC Source." The new FRDC source was supposed to be distributed not only to PTB, JEMIC and ETL, but also to other national standard laboratories which are interested in the use of the FRDC source. A prototype of the new FRDC source was completed in January 1994. After the evaluation and minor change of circuit-design, the production of the new FRDC source has been started in November 1994. Until October 1995, eight FRDC sources have been manufactured, and were distributed to CSIRO/NML, PTB, NIST, KRISS, JEMIC, and ETL.

#### 5.2.1 Designing

One of the main goals in the production model is the realization of fully automated FRDC-DC difference measurement. As shown in the following section, all the control parameters, such as output level, switching frequency, dummy resistance, are remote-controlled through GP-IB interface. In the development of production models, assembly and wiring have been performed by Yatoro Electronics Co. The company was also responsible for the detailed designing of the source including the layout of printed-circuit boards.

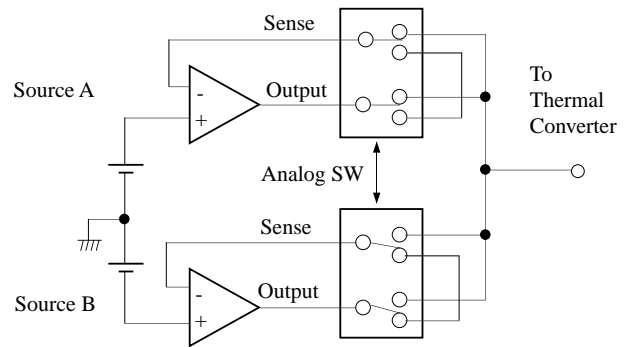
Another important goal in the production model is the realization of voltage-mode output of the FRDC waveform. In the case of evaluation models, the output amplifier was designed as constant current source in order to avoid the effect from the ON-resistance of analog switches. However, it was found that the dependence of the thermoelectric transfer difference on the output modes (voltage or current) can be as

large as a few ppm, as described in section 4.5.2. Consequently, it was determined that the voltage-mode output function should be included in the production model.

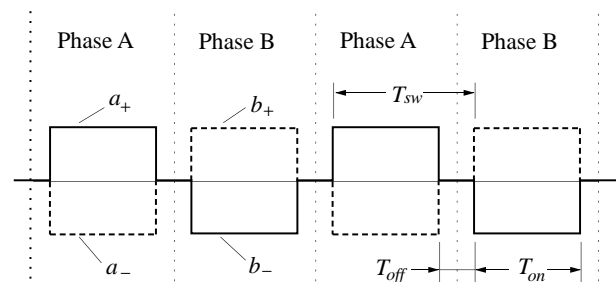
It is not difficult to realize the voltage output by placing a voltage buffer after the switching circuit. Though the finite resistance of the analog switch can be avoided, the voltage buffer might itself become the new source of the memory-effect. Thus, in the production-model FRDC source, an 'external-sense' method is introduced, which is illustrated in **figure 5.1**. In this method, the sense lead is extended over the analog switches in order to avoid the influence of the on-resistance ( $75\Omega$  typ.) of the switching elements. The sense lead is switched simultaneously with the switching of the output circuit.

#### 5.2.2 Waveform-parameters

The waveforms of the new FRDC source are specified by the six parameters as shown in **figure 5.2** and **table 5.1**. The switching period  $T_{sw}$  is defined by a 'base-period' parameter  $T_{base}$  and 'scale-factor' parameter  $m$  as



**Figure 5.1** The voltage output circuit using the 'external-sense' scheme. The sense lead switches simultaneously with the switching of the output circuit.



**Figure 5.2** Parameters of the FRDC waveform. The setting-range of the parameters are listed in the Table 5.1.

**Table 5.1** List of parameters of the modified FRDC waveform.

Parameter	Discription	Range
$\alpha$	Voltage/Current output level	0 to 10.23 (V/mA)
$\beta$	Adjustment for output level	0 to $\pm 2.047$ (%)
$T_{sw}$	Switching Period	0.1ms to 25.5 s
$T_{off}$	Off-Time	4 $\mu$ s to 255 $\mu$ s

$$T_{sw} = T_{base} \times 10^m. \quad (5.1)$$

The parameter  $T_{base}$  can be set in a range from 0.10 (ms) to 2.55 (ms) with 0.01 ms resolution. The scale-factor  $m$  can be set as an integer between 0 and 4. Hence the switching period  $T_{sw}$  can be set in a range between 0.1 ms to 25.5 s. In other words, the switching frequency can be set in a range between 0.04 Hz to 10 kHz. The off-time can be set in a range between 4  $\mu$ s and 255  $\mu$ s with 1  $\mu$ s step.

The parameters  $a_+$ ,  $a_-$ ,  $b_+$ ,  $b_-$  are further specified by a ‘main value’ parameter  $\alpha$  and ‘adjustment’ parameters  $\beta(A_+)$ ,  $\beta(A_-)$ ,  $\beta(B_+)$ ,  $\beta(B_-)$  as,

$$\begin{aligned} a_{\pm} &= \pm \alpha [1 + \beta(A_{\pm})/100] \\ b_{\pm} &= \pm \alpha [1 + \beta(B_{\pm})/100]. \end{aligned} \quad (5.2)$$

The parameter  $\alpha$  is within a range from 0.00 V to 10.23 V in the voltage mode and from 0.00 mA to 10.23 mA in the current mode. The resolution of the setting is 0.01 V and 0.01 mA for voltage and current mode, respectively. The setting ranges of the adjustment parameters  $\beta$  are within  $\pm 2.047$  (%) with 0.001% (10 ppm) resolution.

In the case of the production-model FRDC source which also employs the new switching scheme, it is necessary to set the value of ‘dummy-load’ resistance. The value of the

‘dummy-load’ resistance can be set in a range from 0  $\Omega$  to 1.5 k $\Omega$  with 0.1 k $\Omega$  resolution. In the normal operation, the value is adjusted to the same value as the input-resistance of the thermal converter to be measured.

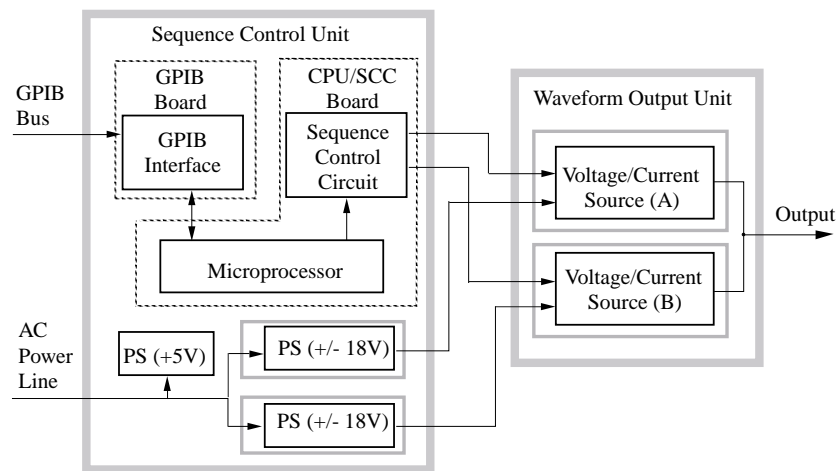
### 5.3 Circuit description

The new FRDC source consists of two separate chassis, i.e., Sequence Control Unit (SCU) and Waveform Output Unit (WOU), for the purpose of isolating the sources A/B and the digital control circuits both electrically and thermally. The schematic diagram of the FRDC source is shown in **figure 5.3**.

The WOU box contains two identical circuits, i.e., the source A and the source B. The two circuits are separately shielded in thick aluminum boxes in order to avoid possible interference between the two circuits. The SCU box contains following three PC boards.

- A CPU/SCC board which generates a control signal and timings.
- A GP-IB Interface board for remote control.
- A dc power supplies for digital control circuits (+5V) and the two sources A/B ( $\pm 18V \times 2$ ).

The two pairs of the optical-fiber lines, which connects the CPU/SCC circuit and the sources A/B, have dual purposes, i.e., for transmission of the timing-signals for the op-



**Figure 5.3** The schematic diagram of the production-model FRDC source. The WOU contains the ‘Source A’ and the ‘Source B’ circuits. The SCU generate a control signal and timings. The optical-fiber lines transmit control signals from the CPU/SCC circuit to the sources A/B.

eration of analog switches, and for sending the commands for controlling the output parameters of the sources A/B.

As described in section 4.4.3, the equality of the rms value between the CPDC modes and MDRF modes is valid on condition that there is no correlation between the outputs of the sources A/B. In order to satisfy this condition and to avoid possible interference between the sources A/B, the optical fiber and isolated power supply has been used in the new FRDC source.

### 5.3.1 Sequence Control Unit

The CPU/SCC is a digital circuit for controlling the operation of the sources A and B. The CPU/SCC circuit consists of six circuit blocks, i.e., Z84C CPU circuit, the Pulse Generator circuit, Parallel-Serial conversion circuit, Optical-fiber Handshake circuit, the A/B Selector circuit, and GP-IB handshake logic circuit. A simplified circuit diagram is shown in **figure 5.4**.

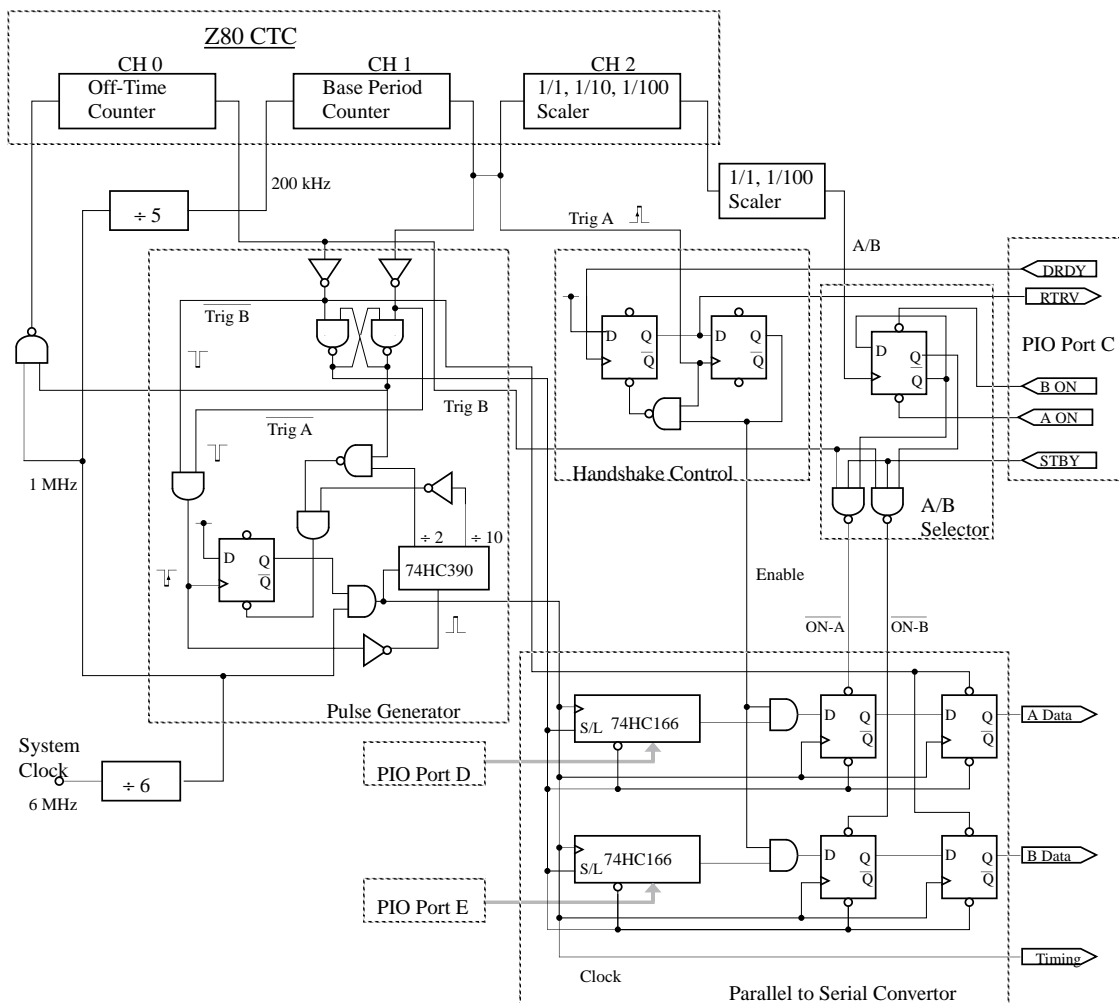
#### (1) Z84C CPU circuit

The Z84C CPU circuit is a single-board computer Model KBC-Z11 from Kyohritu Denshi Sangyo co. A Toshiba

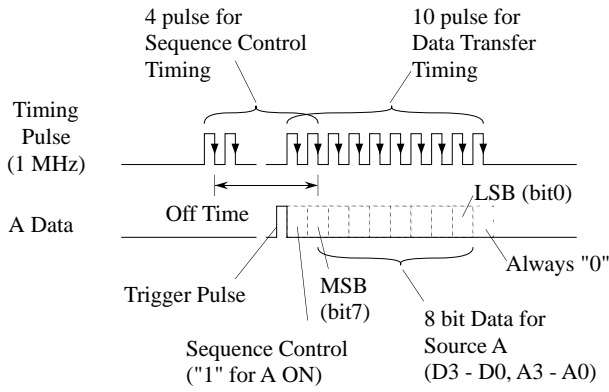
TMPZ84C011AF micro-processor is used as a core unit of the board. The micro-processor includes 6 MHz Z80CPU, five 8-bit programmable I/O ports, and four-channel programmable timer/counter(CTC). The GP-IB handshake logic circuit and the Sequence Control Circuit are controlled via the five I/O ports of the micro-processor. The CTC produces the basic period and timing for the Sequence Control Circuit. The CTC#0 is used to set the 'off-time' in one ms unit. The CTC#1 creates the 'base period' in 5 ms interval. The CTC#2 and the '1/10, 1/100 Scalar' circuit determines the scale factor "m" of the switching period. The EPROM program is described in section 5.3.3.

#### (2) Pulse Generator circuit

The Pulse Generator circuit combines the timing signals ('off-time' and 'base period') from the CTCs, and makes the 'timing-pulse train' for transmission through the optical fiber, as shown in **figure 5.5**. The first four pulses of the timing pulses are used to control the timing for the analog switches in the source A/B circuit. The timing pulses, excluding the first two pulses, are also used to synchronize 'data-



**Figure 5.4** A simplified circuit diagram of CPU/SCC circuit. The CPU/SCC is a digital circuit for controlling the operation of the sources A and B.



**Figure 5.5** The ‘timing-pulse train’ for transmission through the optical fiber. The first four pulses control the switching timing for the analog switches. The ‘data-pulse train’ is used for the transmission of control-data for the source A/B circuits.

pulse train’ which is used for the transmission of control-data for the sources A and B.

(3) Parallel to Serial Conversion circuit

The control-data for setting DACs, mode registers, and relays on the sources A and B are send from the Z80 CPU via the port PD and PE. The Parallel to Serial conversion circuit receives the control-data, which consists of 4 bit address and 4 bit control data, and transmits to the sources A/B as the serial ‘data-pulse train’ through the optical fiber lines.

(4) Optical-fiber Handshake Control circuit

The transmission of the control-data is synchronized to the timing pulse, and one set of data is send through the optical fiber lines during one base-period interval. The Optical-fiber Handshake Control circuit controls the timing for updating the control-data on Port D/E of Z84 CPU, using a hand-shake control by port PC and two flip-flops.

(5) A/B Selector circuit

The A/B Selector circuit controls the switching of the output between the sources A and B. As described in the previous section, the interval of the switching is determined by ‘base-period’  $T_{base}$  and the ‘scale-factor’  $m$ . Hence the switching signal should be send to the sources A/B once in  $10^m$  of the ‘base-period’. The switching signal is transmitted as the second bit in the ‘data-pulse train’, as shown in the figure 5.5.

(6) GP-IB Interface

The FRDC uses general-purpose GP-IB/Parallel I/O interface unit Model UIO-488Z from MCI engineering co. The UIO-488Z receives the GP-IB commands by ASCII format and outputs the ASCII characters to the 8-bit parallel output buffer. A hand-shake cricuit interfaces the UIO-488Z to the Z84C CPU board.

(7) Power Supply

The Power Supply circuit consists of two  $\pm 18$  V/ 200 mA power-supplies for Sources A/B and a +5 V/ 1A power-supply for all the circuit in the Sequence Control Unit. All the power supply circuits use series-regulator circuits to avoid high-frequency noise of the switching-regulator circuits.

In order to reduce coupling between the sources A and B through the power supply, ‘R-cores’, which produce much smaller leakage-flux than the ordinary magnetic cores, are used in the power transformers. Electrostatic shield is inserted between the primary and the secondary winding of the power transformer. In addition, the two  $\pm 18$  V power supplies are separately enclosed in two magnetic-shield boxes made of soft-steel.

5. 3. 2 Waveform Output Unit

The Waveform Output Unit consists of two identical circuits, i.e., the source A and the source B. The circuits of the sources A/B are separately shielded by aluminum boxes with 6-mm wall-thickness. The boxes prevent both the electromagnetic and thermal couplings between the sources A/B.

The sources A and B each consist of the following three PC boards;

- (a) ‘Output I’ board which contains analog switches for synthesizing the FRDC waveform, and a digital control circuit to provide timing-signal for the switches.
- (b) ‘Output I-sub’ board which contains the high-stability dc voltage source and current source.
- (c) ‘Output II’ board which contains voltage regulator circuits and dummy-load circuits.

The schematic diagram of the circuit is shown in **figures 5.6** and **5.7**. The figure 5.6 shows the digital control circuit, and the figure 5.7 shows the analog circuits. Since the two sources A and B are identical, only one of the two sources is explicitly shown in the figure.

(1) Digital control circuit

The digital control circuit has the following dual purposes;

- (a) Receive timing signal from SCU as the ‘timing-pulse train’, and create the switching sequence for the analog switches.
- (b) Receive control-data from SCU as the ‘data-pulse train’, and set DACs, mode registers, and relays for dummy resistance.

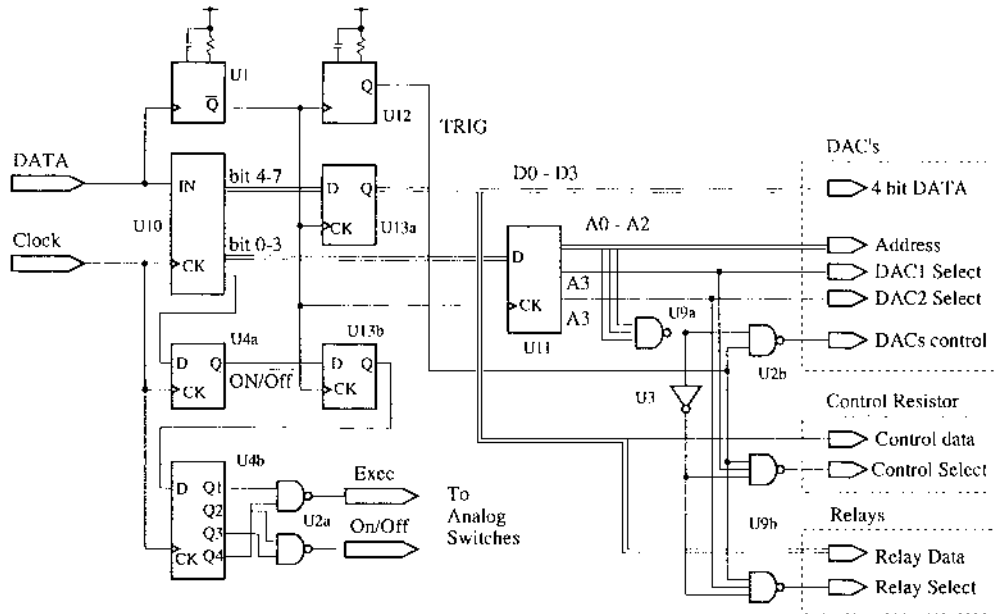
The control data for switching of the output between the sources A and B are send by the second bit of the data-pulse train, and are stored in U13. If polarity of the second bit is reversed, polarity of the analog switch SW6 is reversed in synchronization with the next data-pulse train. The switching sequences for the analog switches are generated by U4 and two NAND gates of U2, synchronized to the first four bits of the timing-pulse train.

The 8-bit control-data, received from the SCU via the optical-fiber transmission line, are converted from serial data to parallel data by U10 and U4. The upper four bits (data-bits) are stored at the data-buffer U13, and the lower 4 bits

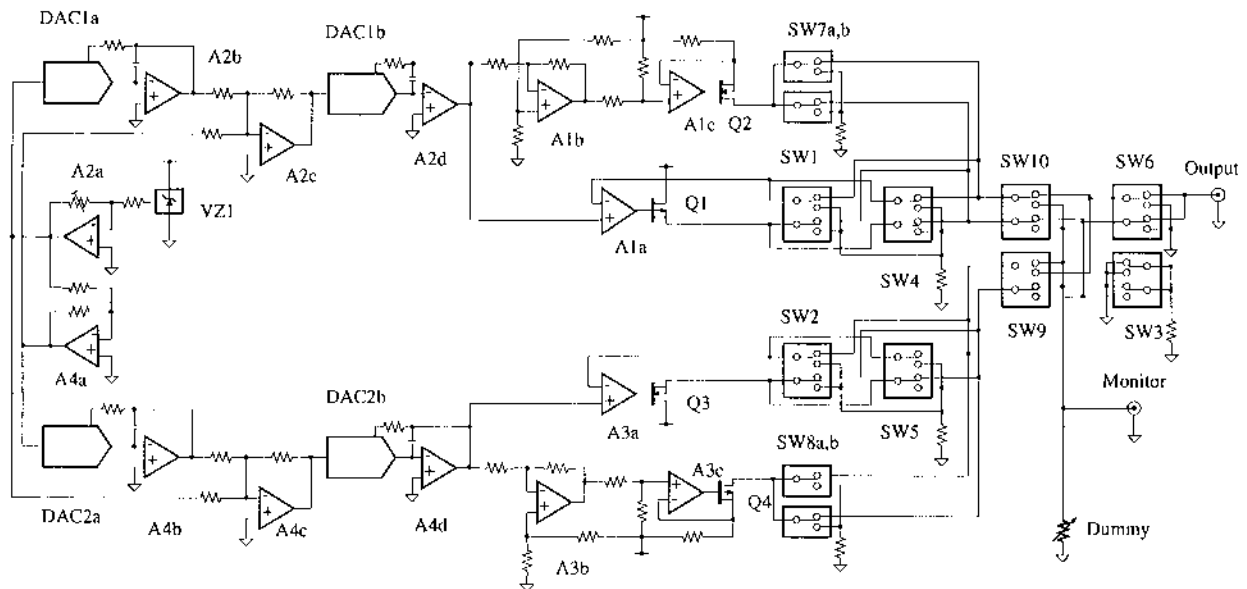
(address-bits) are stored at address buffer U11. The address-bits are decoded by U11, U9, U3 and U2, and corresponding data-bits are sent to either DACs, mode registers, or relay registers for setting dummy resistance. The DACs receives three 4-bit data to specify its 12-bit-resolution output level. The mode register controls the output-mode, and the relay registers determine the values of dummy resistor.

(2) Waveform-synthesis circuit

The waveform-synthesis circuit consists of the high-stability dc sources and a set of analog switches. The circuit generates the two MDFR waveforms and the two CPDC waveforms, according to the control-data and timing-signal from the SCU unit. The output is produced either from a positive-polarity dc source (upper part of the circuit diagram)



**Figure 5.6** The schematic diagram of the digital part of the source A/B circuit. The digital circuit receives the timing signal from the SCU and creates the switching sequence for the analog switches. The digital circuit also controls the set-up for DACs, mode registers, and relays for dummy resistance.



**Figure 5.7** The schematic diagram of the analog part of the source A/B circuit. The circuit consists of high-stability dc sources and analog switches to produce 'Phase A' or 'Phase B' of the FRDC waveforms.

or from a negative-polarity dc source (lower part of the circuit diagram). The switching elements are high-speed CMOS analog switches (IH5143) which have been used in the second evaluation circuit. The zener voltage reference VZ1, combined with the OP amps A2a and A4a produces stable reference voltage of  $\pm 10.00\text{V}$ . DAC1b and DAC2b set the output level by 12-bit resolution. DAC1a and DAC2a adjust the positive output level and negative output level separately, up to  $\pm 2\%$  with 10 ppm resolution. The OP amp - FET combinations A1b/c-Q2 and A3b/c-Q4 are V-I converters for constant current output. Switches SW7 and SW8 generate the MDFR or CPDC waveform at current-output mode. The timing signal for SW7b/SW8b is delayed 100 ns relative to SW7a/SW8a to perform 'make-before-break' operation. As will be described in section 5.4.2, FETs are used in the output amplifier in order to suppress the injection of the bias current to the output. The OP amp - FET combinations A1a-Q1 and A3a-Q3 are voltage buffers for constant voltage output. Switches SW1/SW4 and SW2/SW5 generate the MDFR or CPDC waveform at voltage-output mode. As described in section 5.2.1, the sense lead is switched simultaneously with the switching of the output circuit in order to avoid the influence of the on-resistance of the analog switches. As in the case of current output, the timing signal for SW4 and SW5 are delayed 100 ns relative to SW1 and SW2, in order to perform the 'make-before-break' operation.

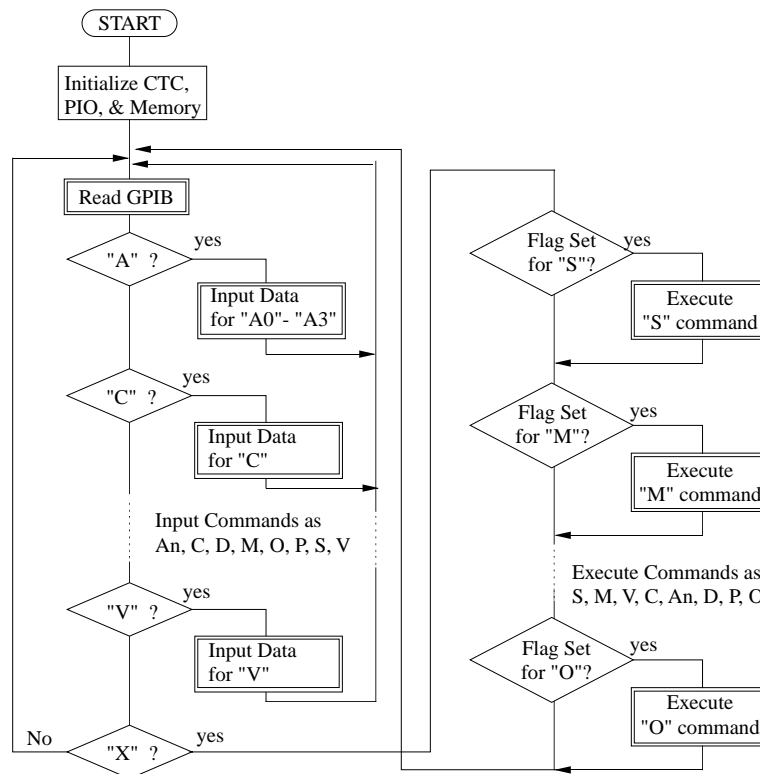
Switches SW9 and SW10 exchange the output from the positive-polarity sources (A+, B+) and the negative-polarity sources (A-, B-) either to the output terminals or to the dummy-resistors. For example, in the case of MDFR[1] waveform, the sources A+ and B- are connected to the output terminal and the sources A- and B+ are connected to the dummy-resistor.

The switch SW6 exchanges the output between the sources A and B. Since the output leads from the switches are regarded as a part of the TC-input circuit, a Teflon printed-circuit board is used in order to avoid the effect from the dielectric loss, as described in detail in section 5.4.3. In order to avoid floating of the output, SW3 connects the output-terminal to the GND during the 'off-time' period.

### 5.3.3 EPROM software

The operation of the FRDC source is controlled by a micro-processor (Z84C) using a program stored in an EPROM. The control program has two modes of operation, namely the command-input mode and the command-execute mode. The simplified flow-chart is shown in **figure 5.8**.

In the command-input mode, the program receives the commands from the system-controller through the GP-IB interface. The list of the GP-IB commands is summarized in **table 5.2**. In this mode, the program continuously watches the 'READY' flag from the GP-IB interface circuit. When



**Figure 5.8** Simplified flow-chart of the control program. The control program has two modes of operation, namely the command-input mode and the command-execute mode. Upon receiving the X-command, the program goes to the command-execution mode.

**Table 5.2** The list of the GP-IB commands.

Function	Format	Description
Voltage Level	V nn.nn	Select Voltage-Output as "nn.nn V"
Current Level	C nn. nn	Select Current-Output as "nn.nn mA"
Adjustment of Output Level	A0 ±n. nnn	Adjust Output Level of A(+) as "±n.nnn %"
	A1 ±n. nnn	Adjust Output Level of A(-) as "±n.nnn %"
	A2 ±n. nnn	Adjust Output Level of B(+) as "±n.nnn %"
	A3 ±n. nnn	Adjust Output Level of B(-) as "±n.nnn %"
Period	P0 n.nn	Set Switching Period as "n.nn ms"
	P1 n.nn	Set Switching Period as "nn. n ms"
	P2 n.nn	Set Switching Period as "nnn ms"
	P3 n.nn	Set Switching Period as "n.nn s"
	P4 n.nn	Set Switching Period as "nn. n s"
Off-Time	O nnn	Set Off-Time as "nnn μs"
Dummy-Load	D n.n	Adjust Dummy-Load Resistance as "n.n kΩ"
Output Sequence/ Mode	M 0	Sequential Output --- AC(1) Mode
	M 1	Sequential Output --- DC(+) Mode
	M 2	Sequential Output --- DC(-) Mode
	M 3	Sequential Output --- AC(2) Mode
	M 4	Steady-State Output --- Source A(+)
	M 5	Steady-State Output --- Source A(-)
	M 6	Steady-State Output --- Source B(+)
	M 7	Steady-State Output --- Source B(-)
Enable/Disable Output	S 0	Disable Voltage/Current Output
	S 1	Enable Voltage/Current Output
Execute	X	Execute Commands

the flag is set, one character (8 bit) is received via PIO port-A using a handshake-procedure. The commands are stored in the command-input buffers in the ASCII format. Upon receiving the X-command, the program goes to the command-execution mode.

In the command-execute mode, the commands stored in the command-buffer are executed one by one in the alphabetical order. The parameters stored in the ASCII formats are converted to four-digits BCD and then to 16-bit binary numbers. Then the data are transferred through the optical fiber lines using a handshake control from PIO port C. After execution is completed, the program returns to the command-input mode.

## 5. 4 Evaluation

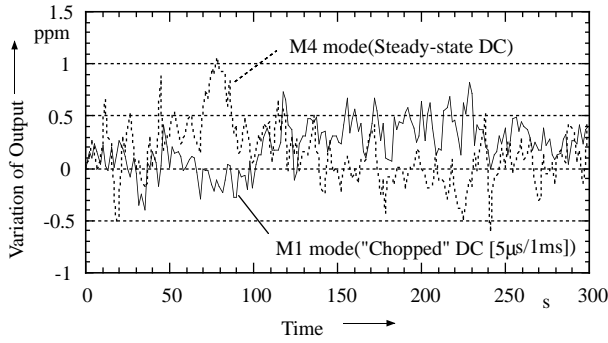
The FRDC-DC difference measurements have been performed using the production-model (KST003) FRDC source to evaluate the uncertainty in the measurement. The results are described in the following sub-sections 5.4.1 to 5.4.5. As in the case of the first and the second evaluation circuits,

K182 nano-voltmeter has been used as a detector of the output EMF from a TCC or TVC. The measurement system and the procedure to determine FRDC-DC difference will be described in detail in chapter 8.

### 5. 4. 1 Stability of the output

There are two kinds of instability in the output of the FRDC source, i.e., the short-term instability (noise) and the long-term instability (drift). For example, jitters of timing pulse due to transmission through optical fiber give rise to random noise in the output rms. The change of temperature in the source A/B circuit causes a drift in the output. Those instability result in the variation of the EMF-output from the TCs, and contribute to the random error in the FRDC-DC difference measurement.

A result of an experimental evaluation for the stability of the output is given in **figure 5.9**. In this measurement, the output voltage was directly monitored by a high-precision DVM (HP3458A). In the case of CPDC waveform which has periodical glitches, a low-pass filter was inserted at the output in order to get the average rms value. As shown in the



**Figure 5.9** Stability of the output of a production-model FRDC source. The output voltage was measured by a high-precision DVM (HP3458A).

figure, the instability of the FRDC source stayed within  $\pm 0.5$  ppm both in the dc mode and CPDC modes.

#### 5. 4. 2 Dependence on the dummy resistance

In the second evaluation circuit, the results of FRDC-DC difference measurements for TCs were found out to be dependent on the value of the dummy resistance. This phenomenon was supposed to be caused by the following processes:

- [1] In the case of new switching scheme, the load resistance of the current-output circuits is switched between a thermal converter and dummy resistors, at the time of mode-switching.
- [2] If the values of dummy resistors are not matched with the input resistance of the TC, the load resistance of the current-output circuits changes with the mode-switching.
- [3] The change in the load resistance causes the decrease or increase in the power dissipated in the output transistor.
- [4] The increase in the dissipated power causes a temperature-rise of the output transistor and results in the enlargement of the current-amplification factor  $h_{fe}$ , which is strongly dependent on the temperature.
- [5] Since the bias current which flows into the output circuit is not compensated by the feed-back loop, variation in the current-amplification factor gives rise to the drift of the output current.

If the drift of the output current is correlated to the mode-switching, the drift is not compensated by the normal measurement sequence (\*+/-/+\*), and may affect the FRDC-DC difference measurement.

To evaluate the dependence of the output current to the temperature of the output transistor, the transistor was heated-up by a soldering iron by touching for 3 seconds. The change in the current was measured to be more than 800 ppm. Then the transistor was replaced with a FET so that no bias current flows into the output. In this case, the change in the output

current was reduced to be less than 1 ppm for the same heat-up condition. After the modification, the dependence of FRDC-DC difference measurements on the dummy resistance was reduced to be within the detection sensitivity (0.1 ppm).

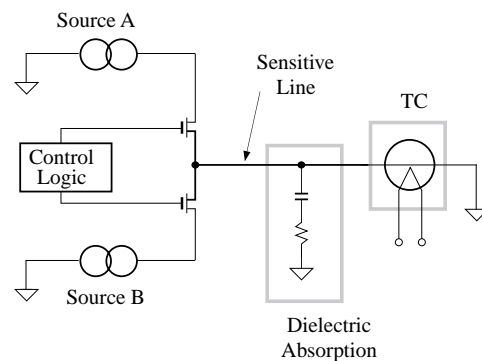
#### 5. 4. 3 Effect of dielectric absorption

When the new FRDC sources were examined using a 10V-range TVC at current mode, a non-negligible error was observed in the FRDC-DC difference at higher frequency ( $>1$  kHz). The error increased linearly with the input-resistance of TC, and the effect was not observed at the voltage mode. This effect was particularly dominant when the ambient humidity was more than 80% or the TC-input circuit was contaminated by finger-print or flux. Hence this effect is supposed to be related to the surface charge or leakage path on the surface of the components. In the worst case, an error of several ppm was observed at 10 kHz with input resistance of 1 k $\Omega$ .

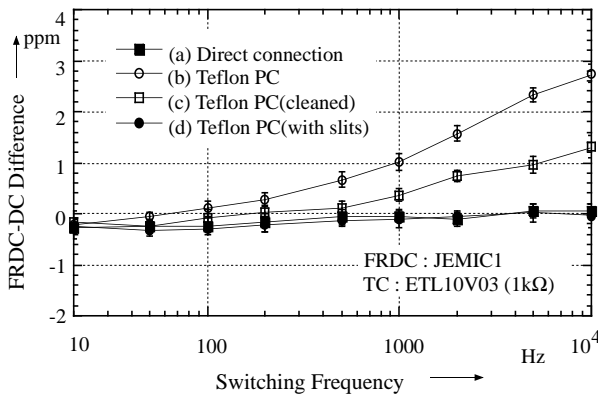
If there is a dielectric loss or dielectric absorption in the insulation between ‘Signal-Hi’ and ‘Signal-Lo’ of the TC-input circuit, as is shown in **figure 5.10**, it can cause frequency-dependent leakage current which affects the FRDC-DC difference measurement. This effect occurs only at the current-output mode, and is proportional to the input-resistance of TC.

The most sensitive circuit includes the print-pattern on the PC board between the output pins of the analog switch (SW6) and the output connector. Hence, several configurations were examined in order to reduce the dielectric effects at the PC board:

- (a) A cable from the output connector was directly soldered to the output pins of the analog switches .
- (b) The analog switches (SW6) were isolated from the main PC board using a pair of small Teflon PC boards.
- (c) The Teflon PC boards were cleaned with organic solvent after soldering the SW6 to the board, in order to remove flux or fingerprints.
- (d) The sensitive print-pattern, which is connected to the



**Figure 5.10** A simplified model for the effect of dielectric loss/absorption in the TC-input circuit. The effect causes frequency-dependent leakage current and affects the FRDC-DC difference measurement in the current-output mode.



**Figure 5.11** The result of FRDC-DC difference measurements for the following output-circuit configurations: (a) direct wiring between the analog switches and the output connector; (b) use of small Teflon PC boards; (c) the Teflon PC boards cleaned with organic solvent, and (d) slits in the Teflon PC boards to isolate most sensitive pattern.

output pin of SW6, were isolated from the other patterns by making slits in the Teflon PC boards.

The result of the FRDC-DC difference measurement for these configurations is shown in **figure 5.11**. As shown in the figure, best performance has been obtained in the configuration (a) and (d), as expected. In these cases, the changes of FRDC-DC difference are within 0.5 ppm at 10 kHz with input resistance of 1 kΩ. The effect reduces below 0.1 ppm for TCCs which have input resistance less than 200 Ω.

The effect of dielectric loss/absorption in the TC input circuit will be quantitatively analyzed using a simple mathematical model in section 6.3.3 .

#### 5. 4. 4 Interference between sources

As described in the previous sections, various precautions were taken to avoid interference between the sources A and B, in order to realize the equality in the rms power between the CPDC and the MDFR modes. In this section, a measurement for the evaluation of the isolation between the sources is described. The method of the evaluation is illus-

trated in **figure 5.12**. The ‘Source A/B Selector’ decompose the waveform and distribute the output from source A or source B to the thermal converter. The output-EMF from the TC are compared for the following four cases.

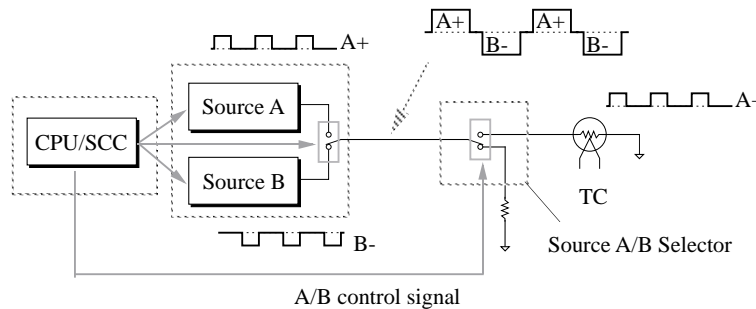
- [1] Apply the positive (A+) output of Source A to the TC and compare the output for the modes between “CPDC+ (A+/B+)” and “MDFR[1] (A+/B-)”.
- [2] Apply the negative (A-) output of Source A to the TC and compare the output for the modes between “CPDC- (A-/B-)” and “MDFR[2] (A-/B+)”.
- [3] Apply the positive (B+) output of Source B to the TC and compare the output for the modes between “CPDC+ (A+/B+)” and “MDFR[2] (A-/B+)”.
- [4] Apply the negative (B-) output of Source B to the TC and compare the output for the modes between “CPDC- (A-/B-)” and “MDFR[1] (A+/B-)”.

In the case [1], for example, the EMF-output from the thermal converter is the same for CPDC+ and MDFR[1] modes on condition that the RMS of the output A+ is not affected by the polarity of the source B. A typical result for such measurement is listed in the **table 5.3**. The measurements were performed at the switching frequencies of 100 Hz and 1 kHz. The difference in the EMF was examined at current mode in order to avoid the effect from the on-resistance of the analog switches. The differences for the eight different configurations were measured to be  $0.02 \pm 0.08$  ppm.

#### 5. 4. 5 Total performance

Among the eight production-model (KST003) FRDC sources which have been manufactured at Yatoro Electronics, six units have been tested using the same reference standard. The standard is a 10-volt range standard TVC (10V03), which has nominal input current of 10 mA with 1 kΩ input resistance. The results of the evaluation are summarized in **table 5.4**. The measured thermoelectric difference for the standard TVC agreed within  $10^{-7}$ . Consistency with the other two FRDC sources (SN#2 and SN#3) is also indirectly confirmed using the another reference standard.

The thermoelectric time constants of the TVC were determined from the frequency characteristic of the FRDC-DC



**Figure 5.12** Schematic diagram of measurement circuit for the evaluation of the isolation between the sources A and B. The ‘Source A/B Selector’ de-compose the waveform to ‘Phase A’ or ‘Phase B’ and distribute the output from the ‘Source A’ or ‘Source B’ to the thermal converter.

**Table 5.3** A result of the evaluation of the isolation between the sources A and B.

Output Modes		100 Hz	1 kHz
Source A+	DC(+) / FRDC(1)	0.00 ± 0.24	-0.11 ± 0.23
Source A-	FRDC(2) / DC(-)	0.13 ± 0.20	0.08 ± 0.26
Source B+	DC(+) / FRDC(2)	0.02 ± 0.18	-0.05 ± 0.19
Source B-	FRDC(1) / DC(-)	0.02 ± 0.20	0.10 ± 0.23
		(ppm)	(ppm)
Date : 95/JUN/14 -- FRDC : JEMIC-1 -- TC : ETL T08			

\* The uncertainty represents one standard deviation for ten measurements.

**Table 5.4** The list of eight production model (KST003) FRDC sources with the results of the total performance test. The reference is a 10-volt range standard TVC (10V03).

#	S/N	user	Time Constant		Thermoelectric Difference	
			10 mA	10 V	10 mA	10 V
1	941001A/B	ETL	0.06 s	0.07 s	-0.27 ppm	-0.50 ppm
2	94B002A/B	NML				
3	954003A/B	NIST				
4	954004A/B	ETL	0.10 s	0.09 s	-0.27 ppm	-0.51 ppm
5	959005A/B	PTB	0.07 s	0.09 s	-0.31 ppm	-0.52 ppm
6	95A006A/B	KRISS	0.05 s	0.09 s	-0.28 ppm	-0.49 ppm
7	95A007A/B	JEMIC	0.07 s	0.09 s	-0.27 ppm	-0.49 ppm
8	95A008A/B	ETL	0.09 s	0.08 s	-0.26 ppm	-0.52 ppm

"Reference TVC : 10V03(10V, 1k $\Omega$ )"

NML : National Measurement Laboratory (Australia)  
 NIST : National Institute of Standards and Technology (USA)  
 PTB : Physikalisch-Technische Bundesanstalt (Germany)  
 KRISS : Korea Research Institute for Standards and Science.  
 JEMIC : Japan Electric Meters Inspection Cooperation

difference measurements. The method to determine the thermoelectric time constants will be described in section 6.2.

## 5.5 Summary

A production-model (KST003) FRDC source has been developed at ETL for the purpose of determining the thermoelectric effects in thermal converters. In this chapter, detailed design of the FRDC source was described. The avoidance of interference between the sources A and B is essential for realizing the equality in the RMS power between the CPDC and the MDFR modes.

For the purpose of estimating the uncertainty in the FRDC-DC difference measurement, the performance of the FRDC source was evaluated on the following items: stability of the output, dependence on dummy resistance, the ef-

fect of dielectric loss/absorption, the interference between the Sources A/B. The estimated uncertainty in the FRDC-DC difference measurement will be discussed in section 8.3.

As an over-all performance test, FRDC-DC difference of a reference TVC was measured using six production-model FRDC sources. The measured thermoelectric transfer difference for the reference TVC agreed within  $10^{-7}$ , which confirmed the reliability of the FRDC method to evaluate thermoelectric effects in thermal converters.